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Recent advances in rolled-up on-chip devices

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ABSTRACT

Planar integrated-circuit architectures, optimized for processing features on two-dimensional wafers, have historically delivered rising density and performance. However, continued planar scaling is increasingly limited by leakage/short-channel effects, escalating power density and thermal constraints, while heterogeneous blocks (passives, logic, sensors, memory, and power) compete for chip area, restricting system-level functional density. Thin-film self-rolling offers a deterministic 3D assembly route that converts planar-fabricated nanomembranes into tubular architectures through strain relaxation after sacrificial-layer release. The resulting 3D microtubes enable drastic footprint reduction, tunable diameter and winding number, and new electrical/optical/magnetic coupling geometries, while retaining strong CMOS compatibility. In this review, we summarize leading fabrication strategies for rolled-up on-chip devices, contrasting external-force-assisted rolling with more controllable internal strain-gradient approaches and comparing wet versus dry release routes for integration yield and manufacturability. We then survey fundamental rolled-up components (capacitors, inductors/transformers, and resonators) and benchmark representative performance against state-of-the-art planar counterparts. Next, we review rolled-up sensors and active devices, spanning integrated FET microtubes, photodetectors, and magnetoresistance sensors, followed by information storage/processing concepts such as tubular magnetic domains and rolled-up racetrack memories. We further discuss rolled-up microenergy devices (supercapacitors and microbatteries) and outline key hurdles, such as ohmic loss, heat accumulation, and packaging, together with emerging mitigation strategies. Looking forward, co-integrating heterogeneous rolled-up building blocks into unified tubular circuits could provide a practical beyond-Moore pathway toward compact, multifunctional electronics. Continued advances in materials, wafer-scale yield, and 3D packaging will be pivotal for translating rolled-up architectures into impactful hardware for sensing, communication, and computing.

1. Introduction

Over the past few decades, integrated circuit (IC) manufacturing has been dominated by planar architectures, as the core semiconductor processes-photolithography, thin-film deposition, etching, and planarization-are intrinsically optimized for defining and processing features on two-dimensional (2D) planar wafer surfaces [1–6]. Historically, this planar paradigm, together with aggressive feature-size scaling, has successfully increased device density and performance. However, as scaling approaches fundamental and practical limits (e.g., leakage and short-channel effects [7–10], escalating power density [11, 12] and thermal constraints [13,14]), the "more Moore" route relying mainly on planar shrink becomes increasingly inefficient [15–17]. Meanwhile, emerging application scenarios, such as next-generation Internet of Things (IoT), fifth-generation/sixth-generation (5G/6G) mobile communication technology, and intelligent edge computing demand higher functional density and compact co-integration of heterogeneous components (passives, logics, sensors, memory, and even power/energy modules) within a constrained footprint [18–21]. In conventional planar layouts, these heterogeneous blocks inevitably compete for chip area, and the achievable system-level integration density is therefore insufficient for the next generation of compact,

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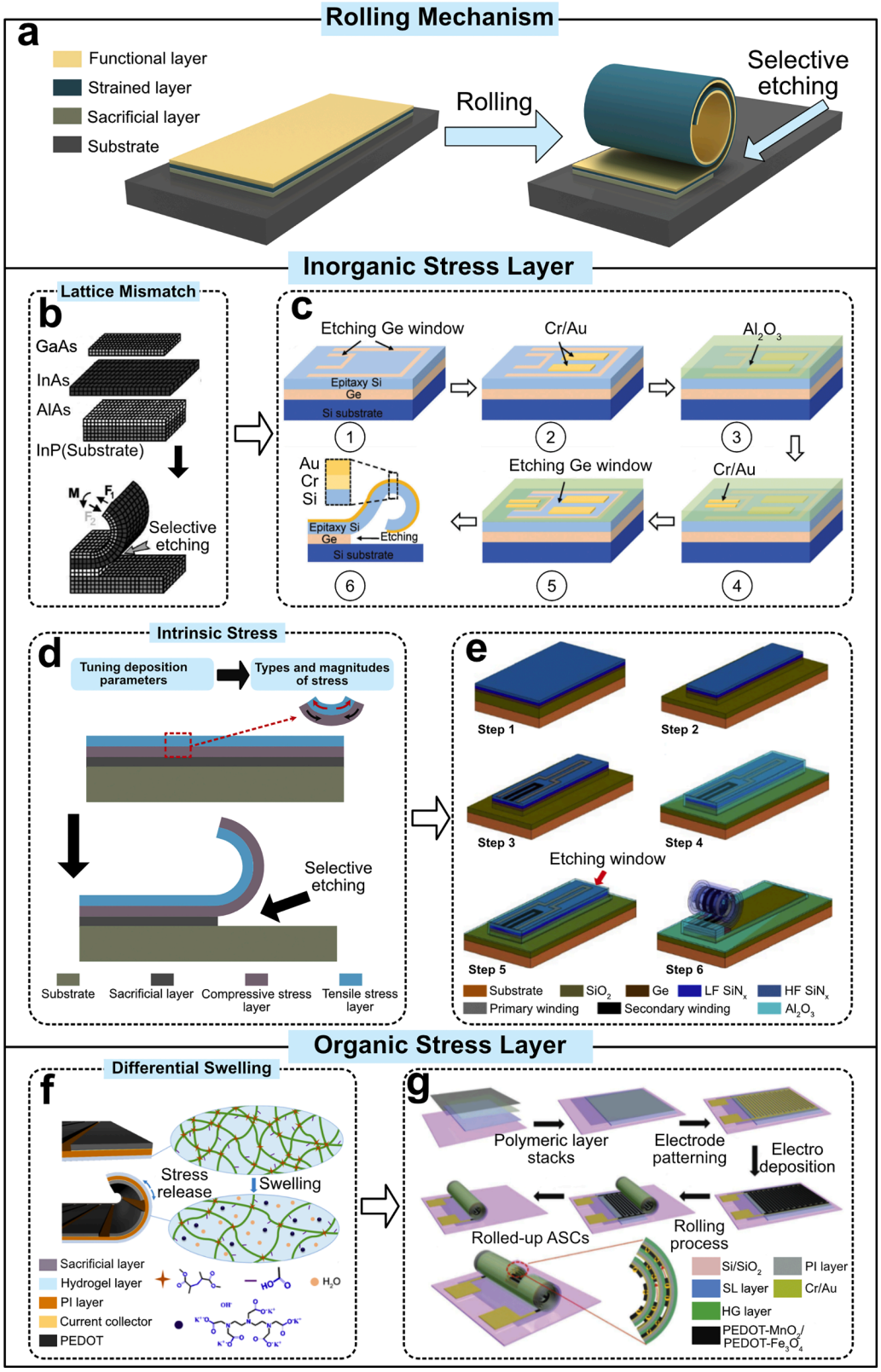

Fig. 1. Three typical mechanisms to achieve rolled-up devices. a, The sacrificial layer, strained layer, and functional layer are deposited sequentially on the substrate, and the sacrificial layer is selectively etched. b, Schematic process to transform a GaAs/InAs bilayer to form a 3D tubular structure. c, Manufacturing steps for a rolled-up 3D tubular Si nanomembrane device. d, Rolled-up process caused by intrinsic stress within the membrane. e, Schematic illustration of the 3D rolled-up transformer fabrication process flow. f, Mechanism of the rolling process caused by hydrogel swelling. g, Schematic illustration of the design and fabrication of rolled-up asymmetric on-chip microsupercapacitors. Reproduced with permission. Copyright © 2003, Elsevier. Copyright © 2019, 2023, Wiley-VCH. Copyright © 2018, Springer Nature. Copyright © 2019, American Chemical Society.

multifunctional electronic systems [18,22].

To overcome the density and footprint bottleneck of planar integration, researchers have developed a variety of three-dimensional (3D) integration strategies. A representative route is die/wafer stacking enabled by through-silicon vias (TSVs) [23–25], which offers high interconnect density and shorter interconnect lengths, benefiting bandwidth and form factor; however, TSV formation and alignment introduce additional cost and yield challenges, and the severe coefficient of thermal expansion (CTE) mismatch between the copper (Cu) and the silicon (Si) [26–30]. Beyond semiconductor stacking, additive manufacturing/3D printing of electronics provides exceptional design freedom and rapid prototyping capability [31,32], but typically suffers from limited resolution, restricted material stacks, and performance gaps compared with complementary metal-oxide-semiconductor (CMOS)-compatible processes [33–35]. In light of these challenges, thin-film rolled-up technology has emerged as an attractive alternative that converts planar-fabricated nanomembranes into 3D tubular architectures [36–40]. By leveraging established planar micro-/-nanofabrication while adding a deterministic 3D assembly step, rolled-up technology can deliver substantial footprint reduction, enable new electrical/optical coupling geometries [41–45], and remain compatible with conventional CMOS technology, making it promising for scalable high-density on-chip integration.

In a typical rolled-up process, a strain-engineered multilayer thin film is first patterned on top of a sacrificial layer using standard planar fabrication. Upon selectively removing the sacrificial layer (wet chemical etching or dry etching), the released nanomembrane relaxes its built-in strain gradient, leading to out-of-plane bending and subsequently rolling into well-defined tubular geometries [46,47]. The resulting tube diameter, winding number, and rolling direction can be engineered through material selection, thickness ratio, strain mismatch, and layout patterning, enabling precise structural control and high repeatability [40,48]. Benefiting from these features, rolled-up 3D microtubular structures have been explored for a broad range of reconfigurable and compact devices, including passive components [39,40,48], transistors [49–52], detectors [43,44,53], sensors [54], and micro-actuators/micromotors [55–57], demonstrating the capability of this approach to build miniaturized, multifunctional 3D on-chip systems beyond the constraints of planar architectures.

In this review, we begin by reviewing the leading fabrication methods for 3D tubular devices, focusing on different strategies to introduce the sufficient rolled-up momentum to the nanomembrane system. Subsequently, we provide a comprehensive overview of fundamental 3D rolled-up basic electronic components, highlighting representative devices and benchmarking their performance against state-of-the-art counterparts. Furthermore, we provide a detailed review of thin-film self-rolling technology in the field of on-chip sensors, such as field-effect transistors (FET) sensors, photodetectors and magnetoresistance sensors. The subsequent section is dedicated to the discussion of 3D rolled-up information storage and processing devices. The discussion in this section primarily includes two parts: the magnetic domain structure in 3D tubular structure and rolled-up domain wall memory devices. This is followed by a detailed review of 3D rolled-up energy storage devices, encompassing rolled-up supercapacitors and batteries. This review concludes by summarizing the critical challenges facing thin-film self-rolling technology in on-chip applications and outlining possible solutions to foster the further advancement of rolled-up 3D on-chip devices.

2. Fabrication processes

In contrast to traditional planar fabrication, the effective utilization of the third dimension significantly expands design freedom, paving the way for enhanced performance and device miniaturization. Among various approaches, 3D rolled-up technology is particularly prominent because it is inherently compatible with established planar semiconductor processing, while offering the integration versatility and structural robustness essential for practical applications. Fundamentally, achieving this tubular geometry requires the generation of a non-zero bending moment within the nanomembranes. This moment is typically introduced via one of two methods: applying external stimuli or engineering intrinsic strain gradients [58,59].

The external force typically acts on the interface of the nanomembrane system, via liquid surface tension [60–62], surface adsorption [63,64], van der Waals forces [65,66], and ultrasonication [67,68]. First, regarding liquid surface tension, approaches such as metal droplet-assisted, solvent evaporation-assisted and solution-based floating technology have been utilized to drive the roll-up process. In metal droplet-assisted methods, following rapid thermal annealing, the metal layer undergoes dewetting to form discrete droplets, and the resulting surface tension, combined with the intrinsic stress of the thin film, drives the rolling process. In solvent evaporation-assisted technology, during the evaporation and drying of solvents such as IPA, a disparity in surface tension between the upper and lower surfaces of the film induces total surface strain and subsequent rolling. For chemically synthesized hydrophobic thin films, when the film floats on a solution surface, the imbalance in surface tension between the gas and liquid phases similarly serves to drive the rolling behavior. Furthermore, in terms of surface adsorption, by exploiting hydrogen adsorption-induced lattice constant modification or lattice distortions resulting from adsorption, adsorption forces induce bending in ultrathin materials, leading to their formation into rolled-up tubular architectures. In addition, as for rolling assisted by van der Waals forces, when a tubular nanowire substrate contacts a thin film floating on a liquid surface, van der Waals forces between the nanowire and the film drive the film to spontaneously wrap around the nanowire, forming a rolled-up tubular structure. Lastly, concerning the ultrasonication rolling method, taking graphene as an example, following the exfoliation of two-dimensional graphene sheets via the reaction of graphite intercalation compounds with solvents such as ethanol, short-duration, high-energy sonication can induce the scrolling of the graphene sheets.

However, the application of external forces has its limitations, primarily attributed to three factors: (i) the lack of precise controllability: external forces such as surface tension, surface adsorption, van der Waals forces, and ultrasound are critically dependent on factors including the interfacial properties and crystal structure of the thin-film materials. Furthermore, these external forces typically operate over broad spatial scales and are subject to a multitude of influencing factors, rendering it difficult to precisely control both the magnitude and the spatial extent of the applied forces. (ii) the complexity of integration with standard semiconductor manufacturing processes: due to the limited precision associated with the aforementioned external force-driven techniques, these methods are unfavorable for the large-scale, high-precision fabrication of integrated devices, and techniques such as liquid-assisted surface tension processes and van der Waals force-induced methods exhibit inherent incompatibility with standard semiconductor manufacturing processes, thereby hindering efficient large-scale processing and fabrication. (iii) the necessity for the continuous maintenance of the external force [36,62–67]: as for certain materials, in the aforementioned external force-driven rolling processes, the rolling of the thin film is primarily induced by external forces. However, since the film itself generates additional internal stress during this process, a competition arises between the external forces and the internal stress. Consequently, continuous application of the external forces is required to maintain the rolled-up state of the thin film.

To the contrary of external forces, introducing internal strain gradients is more controllable, making it highly suitable for the fabrication of 3D on-chip devices. As shown in Fig. 1a, the multilayer thin-film structure for fabricating 3D devices through internal stress gradients is mainly composed of a sacrificial layer, a strained layer, and a functional layer [36,46]. Upon completion of the fabrication of the aforementioned layers on the substrate, the sacrificial layer is removed via selective etching. The released strained film, along with the upper functional

Table 1
Comparison of three types of methods to introduce internal strain gradient.

Mechanism	Typical Materials	Origin of Stress	Advantages	Limitations
Lattice Mismatch	Single-crystal semiconductors (e.g., InGaAs/GaAs, SiGe/Si)	Intrinsic lattice constant difference during epitaxial growth	Provides high-quality single crystals	Requires expensive equipment (e.g., MBE); Material selection is strictly limited to lattice-matched systems.
Intrinsic stress	Amorphous/ Polycrystalline films (e.g., SiN_x, SiO_2, Metals)	Strain gradient induced by varying deposition pressure, power, or frequency (PECVD/Sputtering)	High CMOS compatibility; Applicable to a wide range of materials; radius control.	Materials are often amorphous or polycrystalline, resulting in lower electrical performance compared to single crystals.
Differential swelling	Active materials (e.g., Hydrogels)	Volume expansion/ contraction due to ion intercalation, chemical reaction, or phase transition	Generates large actuation forces; Enables functional devices like energy storage and responsive micro-robotics.	Difficult to precisely control curvature radius.

layer, then rolls up to form a 3D structure. In general, there are several methods to introduce internal gradients. The earliest approach utilized the lattice mismatch existing in epitaxially grown bilayer or multilayer film structures (Fig. 1b). Firstly, rolled-up structures have been successfully fabricated by lattice mismatch induced stress in semiconductor materials ranging from Group IV [69,70] and Group III-V [71] to even Group II-VI [72] compounds. The primary advantage of this method lies in its controllability: since lattice constants are known parameters, researchers can precisely calculate the strain, enabling the rational design of experimental structures [73]. For instance, a Ge epitaxial layer grown on a Si (001) substrate induces a 4% mismatch strain at the interface [58]. In compound semiconductors, the lattice constant varies with composition, allowing for superior strain tuning. This characteristic significantly enhances the controllability of rolled-up micro/nanotubes. Recently, a non-destructive releasing and rolling process has been employed to prepare tubular photodetectors based on freestanding single-crystalline Si nanomembranes [45]. And the spontaneous release and self-assembly process are achieved by residual strain introduced by lattice mismatch at the epitaxial interface of Si and Ge (Fig. 1c). Secondly, beyond costly epitaxial growth, non-epitaxial vapor deposition techniques can also generate strained films [47,58]. Since the strain state is highly sensitive to deposition parameters, the strain gradient can be precisely engineered (Fig. 1d). Recent studies demonstrate the fabrication of 3D tubular electronics by tuning the stress of silicon nitride films via plasma enhanced chemical vapor deposition (PECVD). By optimizing the growth frequency and gas flow rates, the internal stress of the silicon nitride layer can be precisely controlled [74,75]. After selective etching of the sacrificial layer, the released strained film actuates the self-rolling of the upper metallic functional layer, resulting in the formation of specific 3D device architectures (Fig. 1e).

In addition to inorganic materials, organic materials are also capable of rolling up into tubular structures [76,77]. In these systems, the strain gradient typically originates from the differential swelling behavior of polymers with distinct chemical compositions in specific solvents (Fig. 1f). The resulting mismatch in volume expansion between the layers of a bilayer film generates a bending force [76]. As shown in Fig. 1g, some researchers have demonstrated that a novel 3D tubular asymmetric on-chip micro-supercapacitors with a small footprint, high potential window, ultrahigh areal energy density, and long-term cycling stability is fabricated with shapeable materials. This rolling process results from the differential swelling of the hydrogel and the PI film in a designed solution [77]. A comprehensive comparison of the three methods described above is shown in Table 1. Generally, the method of introducing stress via lattice mismatch in epitaxially grown films yields high-quality single-crystal layers, which are highly advantageous for fabricating high-performance semiconductor devices. However, this approach is limited by the high cost of single-crystal growth and a relatively restricted selection of materials. In contrast, non-epitaxial methods, such as PECVD or magnetron sputtering, offer a distinct advantage: full compatibility with mature CMOS processes. This facilitates the scalable fabrication (or mass production) of 3D on-chip devices, although the semiconductor performance of these non-single-crystal films is typically inferior to that of their epitaxial counterparts. Finally, the approach utilizing stress induced by the differential expansion (or swelling) of organic materials can generate large deformations, making it particularly suitable for micro-robotics and energy storage devices [57,77]. Furthermore, 3D tubular devices fabricated from biocompatible organic thin films hold broad application prospects in the field of biotechnology [78,79]. Nevertheless, a significant challenge of this method lies in the precise control of the rolling process.

The fabrication process in rolled-up nanotechnology generally necessitates a detachment step to release the nanomembranes from the substrate, enabling their transformation into 3D architectures. Typically, a sacrificial layer is deposited between the functional nanomembrane and the substrate to facilitate the release of the film. Subsequent lateral etching of this sacrificial layer frees the nanomembrane, thereby triggering the self-rolling process. The etching processes are primarily categorized into wet etching and dry etching. Wet etching is widely adopted for removing the sacrificial layer due to its cost-effectiveness and ease of implementation. The fabrication of rolled-up microtubes was first demonstrated by releasing a strained InAs/GaAs bilayer from an underlying AlAs sacrificial layer [70]. This was achieved by utilizing a dilute HF solution for selective etching. Besides, as shown in Fig. 1c, a 30% H_2O_2 solution was used to remove the Ge sacrificial layer to release the patterned Si nanomembranes, achieving 3D Si nanomembranes based optoelectronic devices [45]. The wet etching is also widely used in the organic strained layer driven rolled-up system. As illustrated in Fig. 1g, the polymeric sacrificial layer is fabricated using acrylic acid (AA) and hydrated $LaCl_3$, and the planar devices roll up into 3D tubular architectures by selectively etching the sacrificial layer in the solution of sodium diethylenetriaminepentaacetic acid (DTPA). Wet chemical etching, while historically ubiquitous due to its high selectivity and isotropic nature, presents inherent limitations for on-chip device integration. The primary bottleneck lies in the deleterious capillary forces generated during liquid evaporation, which frequently induce stiction and structural collapse, thereby compromising device yield [59,80]. Although techniques like critical point drying (CPD) can mitigate this issue, they add complexity to the fabrication process.

In addition to wet etching, thermal release and laser-writing release have long been employed for stress release in thin films. Thermal release relies primarily on high-temperature polymer pyrolysis: after a prestressed thin film is deposited onto a pyrolytic polymer, heating the system to a critical temperature causes the solid polymer sacrificial layer to decompose directly into monomeric gases. This process releases the stress in the overlying film, resulting in the formation of a rolled-up structure [81]. Nevertheless, the stochastic nature of crack formation during pyrolysis in current studies poses a challenge to the directional stability of the rolling process. Laser-writing release is primarily based on either inducing stress gradients via laser irradiation or utilizing lasers to sever the anchors holding the film to achieve rolling. When a laser directly irradiates a polyimide film, the photothermal effect generates a temperature gradient across the thickness, which in turn induces an internal stress gradient; this causes the film to spontaneously detach

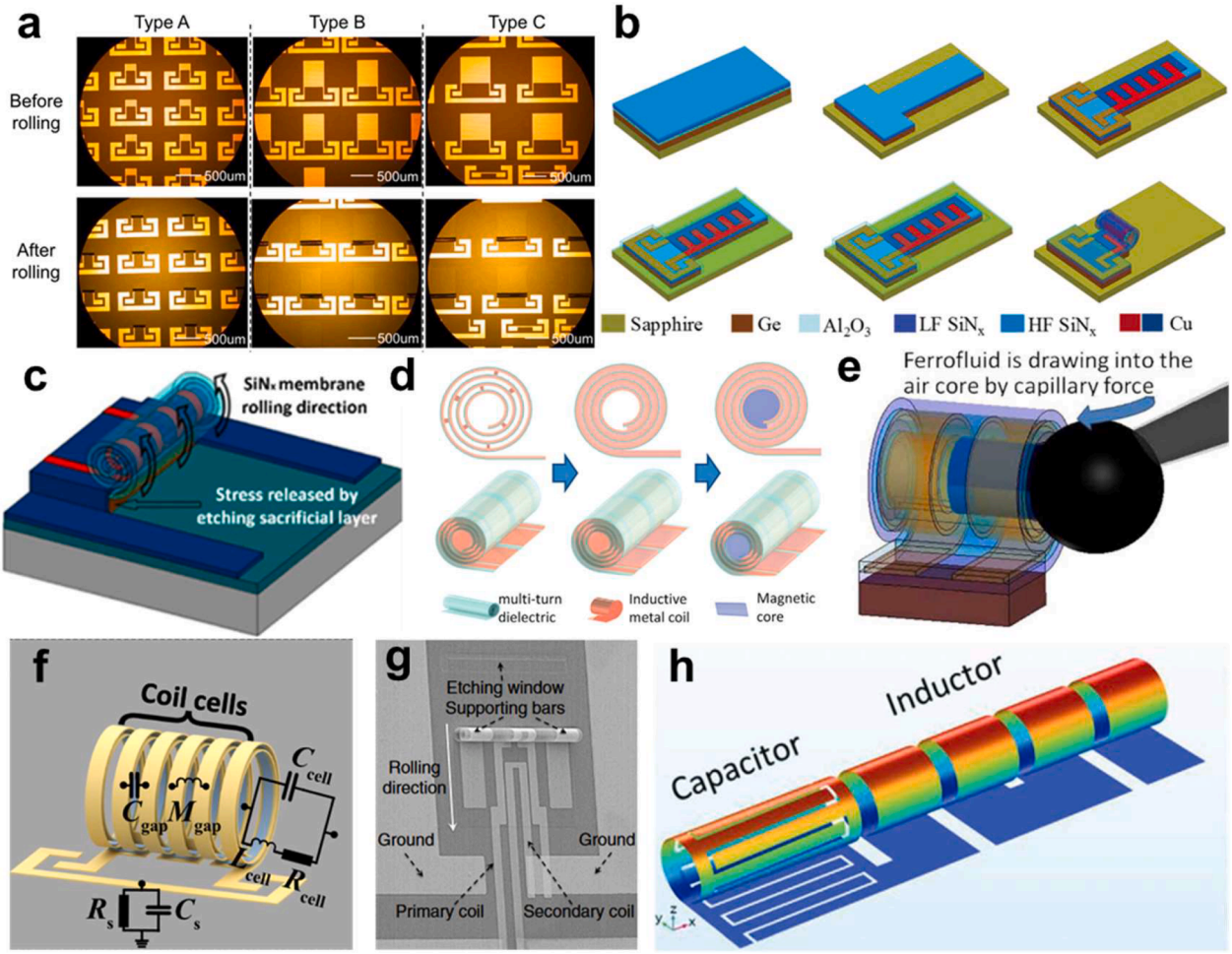

Fig. 2. Rolled-up passive device. a, Optical images of rolled-up interdigital capacitors with different designs (Types A, B and C) before and after rolling. b, (Left) Schematic of the rolled-up interdigital capacitor before and after rolling. (Right) Equivalent lumped circuit model of the rolled-up interdigital capacitor. c, Rolled-up inductor with the membrane releasing mechanism and rolling direction indicated. d, Post-rolling electroplating scheme of rolled-up inductor. e, Post-fabrication capillary core filling scheme of the rolled-up inductor. f, Schematic of the rolled-up magnetic integrated inductor with its equivalent circuit model. g, SEM image of rolled-up transformers, showing the transition of the 2D primary and secondary strips to 3D coils. h, Schematic of the monolithic rolled-up LC resonator. Reproduced with permission. Copyright © 2019, IOP Publishing. Copyright © 2021, IEEE. Copyright © 2012, American Chemical Society. Copyright © 2020, 2024, Wiley-VCH. Copyright © 2020, AAAS. Copyright © 2018, 2025, Springer Nature.

from the substrate and roll up [82]. Additionally, lasers can induce a cross-linking density gradient across the thickness of hydrogel films, thereby introducing a stress gradient that drives the film to spontaneously roll into a tubular structure [83]. For pre-deposited films possessing internal stress, a laser beam can be used to sever the fixing anchors at the film boundaries, releasing the internal stress and leading to the formation of rolled-up microtubes [84]. However, in the aforementioned laser-writing release methods, laser irradiation tends to induce material oxidation, thereby compromising electrical performance. Besides, regarding the rolling of hydrogels, since the process involves the rearrangement of polymer chains, the response speed of the rolling process is inherently limited.

Conversely, dry etching (e.g., vapor-phase etching) avoids liquid-phase interactions, providing a stiction-free release mechanism [36,48,85]. This process not only preserves the structural integrity of the 3D architectures but is also compatible with conventional CMOS technology, which enables its widespread application in the fabrication of rolled-up 3D on-chip devices. For instance, suspended nanomechanical devices can be fabricated by utilizing HF vapor to etch the SiO_2 sacrificial layer [86]. Similarly, SiN_x bilayers (Fig. 1e) and $Al_xGa_{1-x}As$ films can be released to fabricate tubular electronics using gaseous XeF_2 to remove the sacrificial Ge layer [18,87].

3. Rolled-up basic electronic components

The 3D rolled-up technology, an emerging micro-nano manufacturing process, enables the transformation of membranes from 2D planar structures to 3D tubular forms by directing the release of strain energy. Since its inception in 2000, this technique has garnered significant research attention. By integrating 3D rolled-up technology with traditional planar device fabrication processes, researchers have successfully developed a series of miniaturized 3D electronic devices that exhibit performance and size advantages not seen in their 2D counterparts. This opens up new avenues for the integration and enhancement of micro-nano electronic components.

3.1. Capacitors

In modern RF IC, parasitic inductance and resistance from circuit wiring can cause signal disturbance at high frequencies, necessitating the use of RF capacitors for filtering, coupling, and decoupling [88,89]. Due to limited on-chip area, RF capacitors are often required to be compact and have low losses. Compared to traditional planar capacitors, the 3D rolled-up technology allows the planar design to roll into a tubular structure. This increases capacitance through the electric field

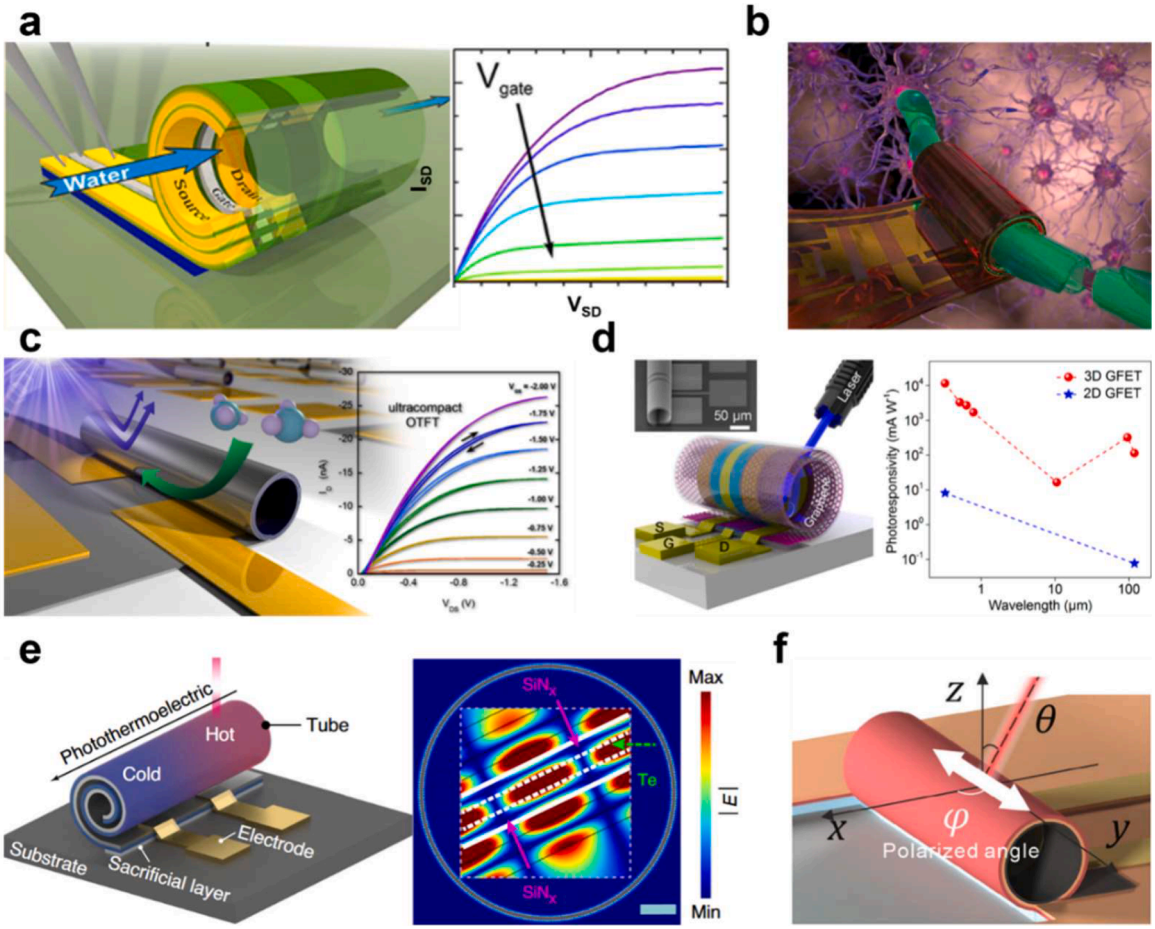

Fig. 3. Rolled-up active device. a, Schematic of the rolled-up transistor for microfluidics (left) and its electrical response (right). b, Schematic of the rolled-up Biomimetic microelectronics. c, Schematic of the rolled-up organic thin-film FET (left) and its electrical response (right). d, (Left) Schematic diagrams of the rolled-up graphene FET; Inset: An SEM of side view of fabricated rolled-up graphene FET, and photoresponses of the rolled-up graphene FET compared with a 2D graphene FET. e, Schematic diagram of the operation mechanism and components of a rolled-up tellurium (Te) thermophotovoltaic photodetector (TTD) (left), and the simulated electric field distribution (right). f, Schematic diagram illustrating the angle of incidence and polarization angle of incident light in a graphene-readout silicon-based Rolled-up photodetector. Reproduced with permission. Copyright © 2013, 2018, 2019 American Chemical Society. Copyright © 2015, 2024 Wiley-VCH. Copyright © 2024, Springer Nature.

coupling between adjacent metallic layers in the tubular structure, while significantly reducing the size of the device. For example, Huang et al. [90] fabricated a rolled-up interdigital capacitor, achieving a capacitance increase of more than 15 times and a capacitance density of 371 pF/mm^2 compared to a planar interdigital capacitor (Fig. 2a). They further developed [91] a lumped equivalent model for the 3D interdigital capacitor, establishing a physical model of the rolled-up interdigital capacitor that includes overlapping capacitance, fringe capacitance, parasitic inductance, and resistance, covering both integer and non-integer turn cases (Fig. 2b). It was demonstrated that the capacitance of the rolled-up interdigital capacitor primarily originates from the overlapping capacitance between interlayer electrodes after rolling, predicting the potential for application in microwave and RF front-end circuits.

3.2. Inductors, transformers and resonators

With the development of modern electronic systems towards higher frequencies and greater integration [92–94], the integration of RF front-ends, energy conversion, and sensors has seen significant progress based on the 3D rolled-up platform. Although Micro-electromechanical Systems [95–97] and advanced packaging technologies like TSV and 3D-IC [98–100] have achieved "quasi-three-dimensional" structures, these methods still rely on costly deep etching technologies or complex multi-layer deposition, which are expensive and lack design flexibility. Recently, Huang et al. [101] proposed the use of 3D rolled-up processes to fabricate 3D rolled-up inductors (Fig. 2c). These inductors, fabricated by stress-induced rolling with dual-layer SiN_x membranes, minimize substrate losses by being elevated from the substrate, significantly reducing occupied area and enhancing inductance density. However, due to the rolling stress, the metal wiring in the inductor is typically thin, resulting in high DC resistance and low Q-factor. To address this, Li et al. [102] proposed a strategy to further electroplate copper and magnetic cores (Ni-Fe permalloy) on the cylindrical structure of the rolled-up inductor (Fig. 2d), achieving a tenfold reduction in resistance. This technique can be referenced for the fabrication of high-Q 3D rolled-up devices.

Filling magnetic cores is one of the main methods to improve the performance of inductors. As shown in Fig. 2e, Huang et al. [39] proposed a 3D rolled-up magnetic-core inductor based on a 3D rolled-up technology, in which a magnetic fluid is injected into the rolled structure as the magnetic core via capillary action. The hollow microtube structure formed by the rolled-up process provides an advantage for magnetic core filling - the magnetic fluid can be drawn into the tube by capillary forces, achieving strong electromagnetic induction. The inductance of a single magnetic-fluid-filled 3D rolled inductor reaches 1.24 μH at 10 kHz, with an inductance area density of 3 μH/mm^2. Cui et al. [48] further proposed a CMOS-compatible 3D rolled-up magnetic

integrated inductor structure (Fig. 2f), in which integrated laminated magnetic thin films are rolled together with the metal layers to achieve efficient 3D magnetic integration. They found that this integration approach significantly enhances the magnetic coupling efficiency between adjacent metal layers in the 3D rolled inductor, causing the inductance area density to increase superlinearly with conductor length. Ultimately, they achieved about 92% yield on a 2-inch wafer. The devices can either be monolithically integrated with other circuit components (such as capacitors, resistors, and transistors) to form functional circuits or modularly integrated with other device units through laser cutting. By optimizing the magnetic multilayers, rolling stress, and geometric parameters of the inductor, the device achieved an inductance area density of 8333 nH/mm^2 at 0.55 GHz, which is nearly two orders of magnitude higher than that of conventional planar inductors.

Further, Huang et al. [40] extended this approach to create 3D rolled-up transformers using multi-layer nested rolls. By rolling the primary and secondary coils into the same tubular structure, they achieved strong magnetic coupling while reducing the dielectric loss associated with traditional planar transformers (Fig. 2g). The resulting 3D rolled-up transformer exhibited a coupling coefficient of up to 0.95 and a reduction in area by approximately 90%, significantly improving performance compared to planar RF transformers. By coupling rolled inductors with capacitors to form 3D LC circuits, Li et al. [41] fabricated a 3D rolled-up LC resonator, achieving a tenfold reduction in area compared to planar LC resonators (Fig. 2h), while maintaining stable performance at high frequencies, providing a feasible solution for millimeter-wave front-end integration.

4. Rolled-up sensors

FETs provide unique advantages and applications in miniaturized electronic detection and sensing, facilitating the development of more sensitive, specific, and robust sensors [103–106]. 3D tubular architectures integrated with FETs exhibit exceptional performance in applications such as microfluidic detection, biological signal sensing, and electromagnetic wave detection, thereby demonstrating the unique capabilities of FETs within such structural configurations. In addition to FETs, 3D rolled-up technology also demonstrates unique advantages in the fields of photodetection and system integration. These 3D photodetectors enable the acquisition of multidimensional detection information and exhibit superior detection performance, all within a reduced on-chip footprint.

Magnetic materials have long been integral to information technology, owing to their stable magnetic states that ensure robust and reliable device operation under ambient conditions. With the discovery of various spintronic effects-including anisotropic magnetoresistance [107–110], giant magnetoresistance [111–114], tunnel magnetoresistance [115–118]-devices based on magnetic materials have undergone rapid development and maturation. Specifically, magnetic field sensors leveraging magnetoresistive effects, characterized by their low cost, high sensitivity, and high reliability, have established themselves as long-standing and mature solutions for magnetic sensing [119–121]. In 3D rolled-up architectures, the rolling process exerts a notable influence on both magnetoresistance and the critical temperature of magnetoresistance [122–124]; furthermore, as 3D systems, these architectures offer specific advantages in sensing performance [38].

Collectively, these unique properties underscore the specific impact of 3D rolled-up architectures on FET sensors, photodetectors and magnetoresistance sensors, highlighting the substantial research prospects and application potential of 3D rolled-up sensing devices.

4.1. Integrated FET microtubes

3D rolled-up integrated FET structures offer a novel flexible electronics platform. With their unique 3D rolled structures, high surface area, and excellent mechanical flexibility, they provide new opportunities for high-performance sensing and microsystem integration. This section reviews the progress of rolled integrated FET microtubes in integrated 3D electronic systems, optical detection mechanisms, and chemical/biological sensing applications. In 2013, Oliver et al. [37] first achieved a 3D rolled-up inorganic FET based on InGaAs/GaAs strained layers (Fig. 3a), with a minimum tube diameter of 5 μm. The rolled-up FET not only maintained the high switch ratio ($> 10^5$) and low subthreshold swing (160 mV/dec) of conventional 2D thin-film transistors, but also formed natural microfluidic channels in the structure, enabling liquid sensing. In 2015, they [78] further developed a 3D rolled-up microelectronic system integrating front-end amplifiers and logic circuits (Fig. 3b). This system, based on IGZO thin-film transistors and 3D rolled-up technology, exhibited amplification functionality with a unit gain frequency of 30 kHz and basic logic unit functions (NOT, NAND), with mechanical adaptability and biocompatibility. With the rise of organic FETs, the compatibility of 3D self-rolling platforms with organic semiconductors makes 3D rolled organic FETs a viable option. As shown in Fig. 3c, Carlos et al. [50] reported a 3D rolled-up organic thin-film FET (r-OTFT) based on organic semiconductors (CuPc), which exhibited low operating voltage (< 2 V) and high stability, with mobility comparable to planar devices. The rolled-up organic FETs offered the advantage of self-packaging, providing resistance to ultraviolet light and chemical gases, compared to planar devices. In 2019, Liu et al. [125] demonstrated the first 3D rolled-up graphene FET (3D-GFET) and applied it in broadband optical detection (Fig. 3d). The tube-like resonant microcavities of the 3D-GFET enhanced light fields and increased the interaction area between light and graphene, enabling detection from ultraviolet to terahertz (THz). The 3D rolled-up GFET demonstrated a photoresponsivity exceeding 1 A/W in the ultraviolet and visible light bands, three orders of magnitude higher than 2D GFETs, and response values of 16.4 mA/W and 0.232 A/W in the mid-infrared and terahertz bands, respectively, with a THz responsivity seven orders of magnitude higher than that of 2D antenna-coupled graphene detectors, while maintaining a high-speed response with a bandwidth of > 1 MHz.

4.2. Rolled-up photodetectors

3D rolled-up tubular structures possess unique geometric configurations, which enable superior optoelectronic detection performance when employed as geometric optical devices. By constructing 3D rolled structures, it is possible to overcome the light absorption limitations of planar materials, effectively control the light field, and promote the development of devices from single-function components to on-chip systems and flexible platforms. To address the issue of limited light absorption path and constrained photothermal conversion efficiency in traditional planar photonic materials, manipulating the light and thermal fields through 3D geometric structures is an effective way to enhance detector performance [126–128]. Huang et al. [43] developed a 3D rolled-up tellurium (Te) thermophotovoltaic photodetector (TTD) using the 3D rolled-up process, achieving a two-order-of-magnitude increase in photovoltage responsivity through light capture of the rolled-up structure and thermal localization effects (Fig. 3e). This device achieved a maximum photovoltage responsivity of 252.13 V/W under illumination, a detectivity of 1.48×10^{11} Jones, and exhibited wide-angle and polarization-dependent detection performance. Mei et al. [129] demonstrated a graphene-readout silicon-based 3D rolled-up photodetector for omnidirectional Mbps-level visible light communication reception. By integrating a graphene-semiconductor material system, the device achieved efficient light absorption and rapid photogenerated carrier readout, with a response speed of 75 ns and a responsivity of 6803 A/W. As shown in Fig. 3f, the microtube structure enabled omnidirectional light capture and enhanced polarization detection, with a data rate of 778 Mbps in visible light communication systems and a field of view of 140°

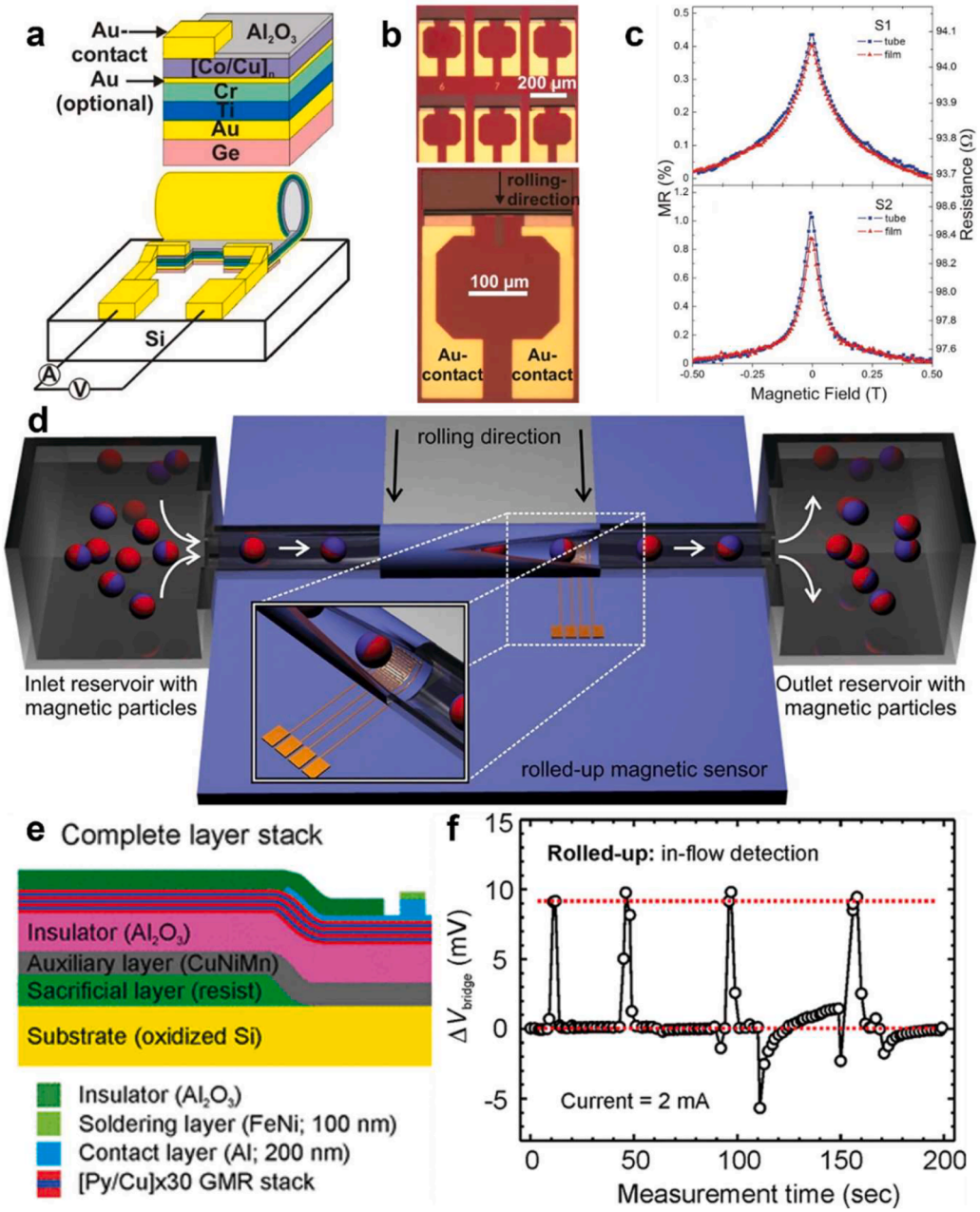

Fig. 4. a, Schematic illustration of the device structure used for investigating magnetoresistance in rolled-up tubular architectures. b, Optical microscopy images of the rolled-up devices. c, Comparison of the magnetoresistive responses exhibited by the devices in planar and rolled-up configurations. d, Schematic illustration of a rolled-up tubular GMR sensor. e, The complete thin-film layer stack of the rolled-up GMR sensor. f, Time-dependent voltage signal of the rolled-up GMR sensor during in-flow detection. Reproduced with permission. Copyright © 2012, AIP Publishing. Copyright © 2011, American Chemical Society.

4.3. Rolled-up magnetoresistance sensors

Magnetoresistive devices based on planar architectures have found mature applications in the fields of magnetic storage and sensing, with their performance characteristics and modulation mechanisms having been extensively investigated [113,116,118]. However, as planar fabrication processes approach their physical limits, the further scaling down of individual planar magnetoresistive devices becomes increasingly difficult. Consequently, on-chip device density is reaching saturation, impeding further enhancement. To transcend the density limitations inherent to planar configurations, 3D architectures, such as rolled-up structures, have been developed and deployed. These 3D rolled-up structures enable higher on-chip device densities; simultaneously, the rolling process introduces additional stress into the constituent magnetic thin films, inducing distinct anisotropies and geometry-dependent critical temperatures. Furthermore, the tubular configuration of 3D rolled-up structures naturally forms microfluidic channels. Integrated giant magnetoresistance (GMR) devices within these channels can effectively achieve high-sensitivity detection of magnetic particles, thereby facilitating compatibility with specialized application scenarios such as in-flow fluidic detection. In 2012, the electrical properties of Co/Cu magnetoresistive devices integrated into 3D tubular structures were first investigated [123]. In this study, a GMR functional layer was deposited onto a stress-driving layer; following the etching of the sacrificial layer and the subsequent relaxation of stress (Fig. 4a), the GMR layer transformed from a planar configuration into a 3D rolled-up tubular structure (Fig. 4b). GMR measurements indicated a 20% enhancement in magnetoresistance for the rolled-up devices

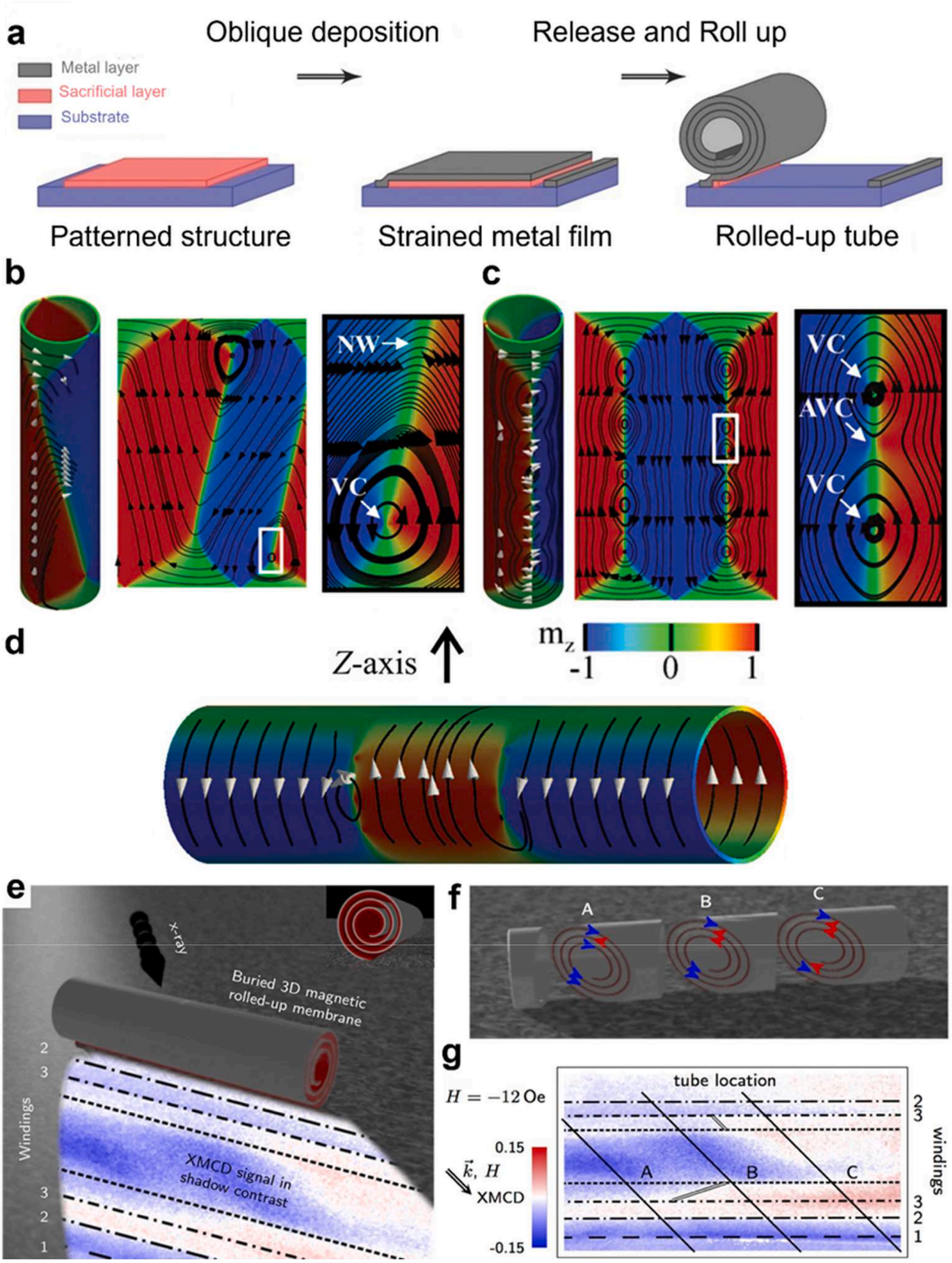

Fig. 5. Magnetic Domain Characteristics in Rolled-up Architectures. a, Schematic illustration of the device used for investigating magnetic domain structures in rolled-up tubular architectures. b, Random distribution and c, A predefined two-domain state of rolled-up permalloy domain structures. d, Domain structures of rolled-up nickel films. e, XMCD characterization of magnetic materials within tubular structures. f, XMCD images of different windings in the rolled-up system under varying external magnetic fields. g, Corresponding magnetic domain patterns. Reproduced with permission. Copyright © 2013, Wiley-VCH. Copyright © 2014, American Chemical Society.

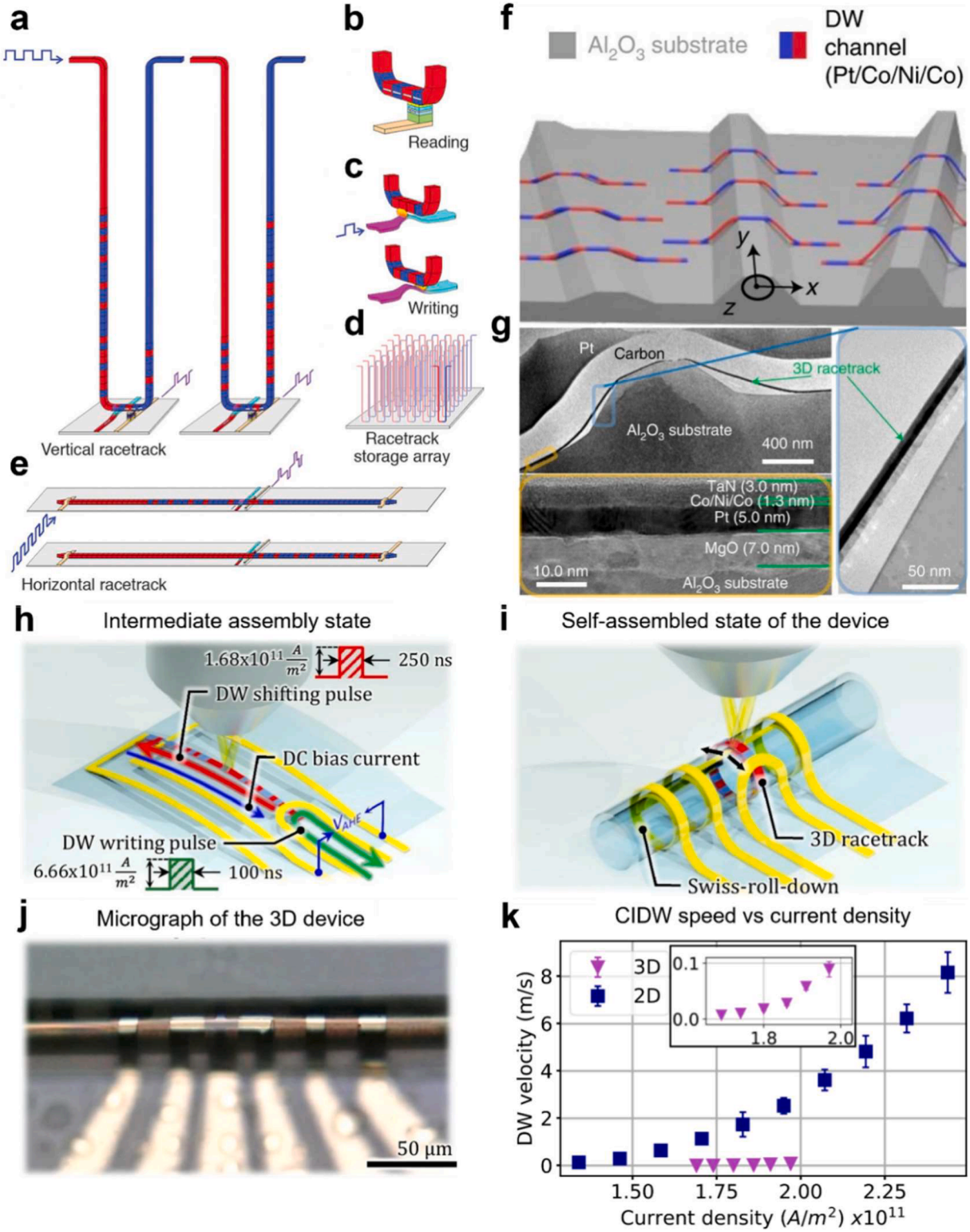

Fig. 6. a-e, Conceptual illustrations of domain wall memory applications, featuring a vision for 3D magnetic storage devices. f, Schematic illustration of 3D memory devices fabricated via MEMS thin-film transfer. g, A cross-sectional electron microscopy image of the 3D structure. h-k, Rolled-up 3D domain wall memory. h, Operational principle of a rolled-up 3D tubular domain wall memory. i, Schematic illustrations of the 3D tubular structure. j, The optical microscope image of the rolled-up device. k, Comparison of domain wall velocities in planar and rolled-up devices under varying current densities. Reproduced with permission. Copyright © 2008, AAAS. Copyright © 2022, 2024 Springer Nature.

compared to their planar counterparts (Fig. 4c). This improvement was attributed to potential factors such as magnetic coupling between adjacent turns, strain-induced electron scattering, and variations in the effective area of current paths within the rolled geometry. Furthermore, within the same material system, it was demonstrated that GMR performance could be further modulated by tailoring the rolled-up geometry through the adjustment of parameters such as the strain state of the Cr layer and the thickness of the Cu layer [124]. Beyond the magnitude of magnetoresistance, the rolled-up architecture also influences the critical temperature of magnetoresistance [38]. Utilizing an InGaAs--Fe_3Si stack, researchers achieved a tubular structure via stress relaxation following the removal of an AlAs sacrificial layer. Temperature-dependent magnetoresistance measurements revealed that the rolled-up Fe_3Si devices exhibited a higher critical temperature compared to planar devices, suggesting that the strain and geometric constraints introduced by the rolling process effectively altered the state of spin disorder within the material.

Magnetoresistive devices are well-established in fields such as magnetic field sensing; however, the integration of these devices with 3D architectures, such as self-folding micro-cubes [130], holds significant potential for 3D vector magnetic field information sensing. 3D magnetic field sensing enables the 3D spatial mapping of static magnetic vector fields and the real-time tracking of moving magnetic objects, thereby finding applications in emerging fields such as electronic skins. Such 3D magnetic spatial perception technologies vividly demonstrate the novel application prospects that 3D architectures offer for magnetoresistive devices.

3D rolled-up structures possess micro-scale tubular geometries that naturally function as microfluidic channels. Furthermore, the integration of GMR devices into the channel walls enables the simultaneous realization of microfluidic transport and magnetic fluid sensing functionalities [37]. Researchers have utilized planar CMOS processing techniques to fabricate planar GMR devices alongside thin-film structures exhibiting a strain gradient. The subsequent release of these films induced self-rolling into 3D tubular structures, resulting in microfluidic channels integrated with GMR sensors (Figure 4d, e). The sensing performance within these tubular configurations is comparable to that of planar devices, indicating that the rolling process does not compromise device functionality. Moreover, these integrated systems demonstrate high-sensitivity detection of magnetic particles flowing through the channels (Fig. 4f). Collectively, these 3D rolled-up GMR devices demonstrate the technical efficacy of this architecture in microfluidic detection applications and highlight the potential of GMR devices within rolled-up systems for 3D, miniaturized, and high-density integration.

5. Rolled-up information storage and processing devices

In ferromagnetic materials, there exist internal regions characterized by uniform magnetization intensity, known as magnetic domains. Magnetic domains are intimately linked to factors such as crystal structure and the alignment of atomic magnetic moments. Consequently, when magnetic thin films undergo a planar-to-3D transformation-such as the rolled-up process-that affects the crystal structure, the magnetic domain structure exhibits significant changes [137–140]. Regarding planar magnetic domain architectures, magnetic disk storage technologies based on these structures have been developed as mature solutions for large-capacity data storage, owing to their high stability, non-volatility, and cost-effectiveness [120–122]. However, these planar storage technologies necessitate a continuous expansion of the physical disk area to increase capacity under limited information storage densities, thereby consuming significant space within circuit systems. To achieve higher magnetic domain storage densities and reduce the spatial footprint of memory devices within systems, 3D storage schemes, such as rolled-up structures, have garnered significant attention from researchers [133,135,136].

5.1. Magnetic domain in 3D rolled-up structures

The structure and dynamics of magnetic domains and domain walls are pivotal to the development of magnetic information storage devices. In 3D rolled-up systems, the unique geometric architecture induces distinct configurations and performance alterations in both magnetic domains and domain walls (Fig. 5a). The 3D rolled-up process introduces additional stress into the constituent magnetic thin films, such as Fe-rich permalloy and nickel films, inducing strain and associated alterations in magnetic domains. Simultaneously, within the rolled-up architecture, additional interactions exist between adjacent tube walls, further influencing magnetic domain properties. Furthermore, this distinct geometric configuration exhibits a specific anisotropic response to magnetic fields [137,140]. Regarding the impact of stress, the stress-induced strain triggers the inverse magnetostrictive effect. Consequently, the angle of Neel-type domain walls significantly decreases after rolling, manifesting as an expansion of the domain wall region. Moreover, magnetic thin films with opposite signs of magnetostriction coefficients-specifically Fe-rich permalloy and nickel films-exhibit distinct orientations of magnetic moments. Concerning the additional interactions between adjacent tube walls, compact wall configurations lacking intermediate insulating interlayers exhibit supplementary interlayer magnetostatic interactions; notably, an increase in the number of wall layers corresponds to an increase in the coercivity of the magnetic material. Additionally, within this unique geometric configuration, magnetic thin film devices possess specific angular anisotropy, demonstrating a distinct anisotropic magnetoresistance response to in-plane magnetic fields applied at varying angles. Distinct from Fe-rich permalloy and nickel film systems, Co/Pt thin films possess magnetic moments with perpendicular magnetic anisotropy (PMA). When integrated into a rolled-up system, these films exhibit a distinctive radial magnetic configuration, establishing a technical foundation for rolled-up magnetic storage devices utilizing perpendicular anisotropy [139]. To further investigate 3D rolled-up systems and elucidate magnetic structural information within complex 3D geometries, researchers have developed a characterization technique based on transmission X-ray magnetic circular dichroism (XMCD) photoemission electron microscopy (PEEM) [138] (Fig. 5e). This method enables the retrieval of local magnetic microstructure information within the 3D architecture through shadow contrast analysis. This approach successfully verified the magnetostatic coupling between different layers of compact tubular walls and characterized tilted domain walls and continuous magnetic domain structures in rolled-up devices containing insulating interlayers (Fig. 5f, g). Thus, it presents an effective characterization methodology for 3D tubular magnetic devices and provides a technical basis for acquiring magnetic information in complex 3D structures.

5.2. Rolled-up domain wall memory

To achieve higher magnetic storage performance, novel spintronic devices such as domain wall memory technology have been proposed [136]. Domain wall memory technology stores bit information utilizing magnetic domains with distinct magnetic moments; electric currents drive the motion of domain walls (Fig. 6a), effectively moving the information-carrying domains past write and read heads to facilitate data writing and readout (Fig. 6b). When an electric current flows longitudinally through heavy metals such as Pt or Ta, the spin Hall effect (SHE) is generated at the upper and lower interfaces of the heavy metal. In heterostructures where magnetic materials possessing PMA, such as CoFe or CoFeB, are vertically stacked with these heavy metals, the SHE induces a spin current that is injected into the magnetic layer. Subsequently, via spin-orbit coupling, this spin current alters the orientation of the magnetic moments, resulting in the displacement of magnetic domains and domain walls, thereby achieving current-driven domain wall motion [131,132].

Furthermore, to achieve information reading and writing, GMR

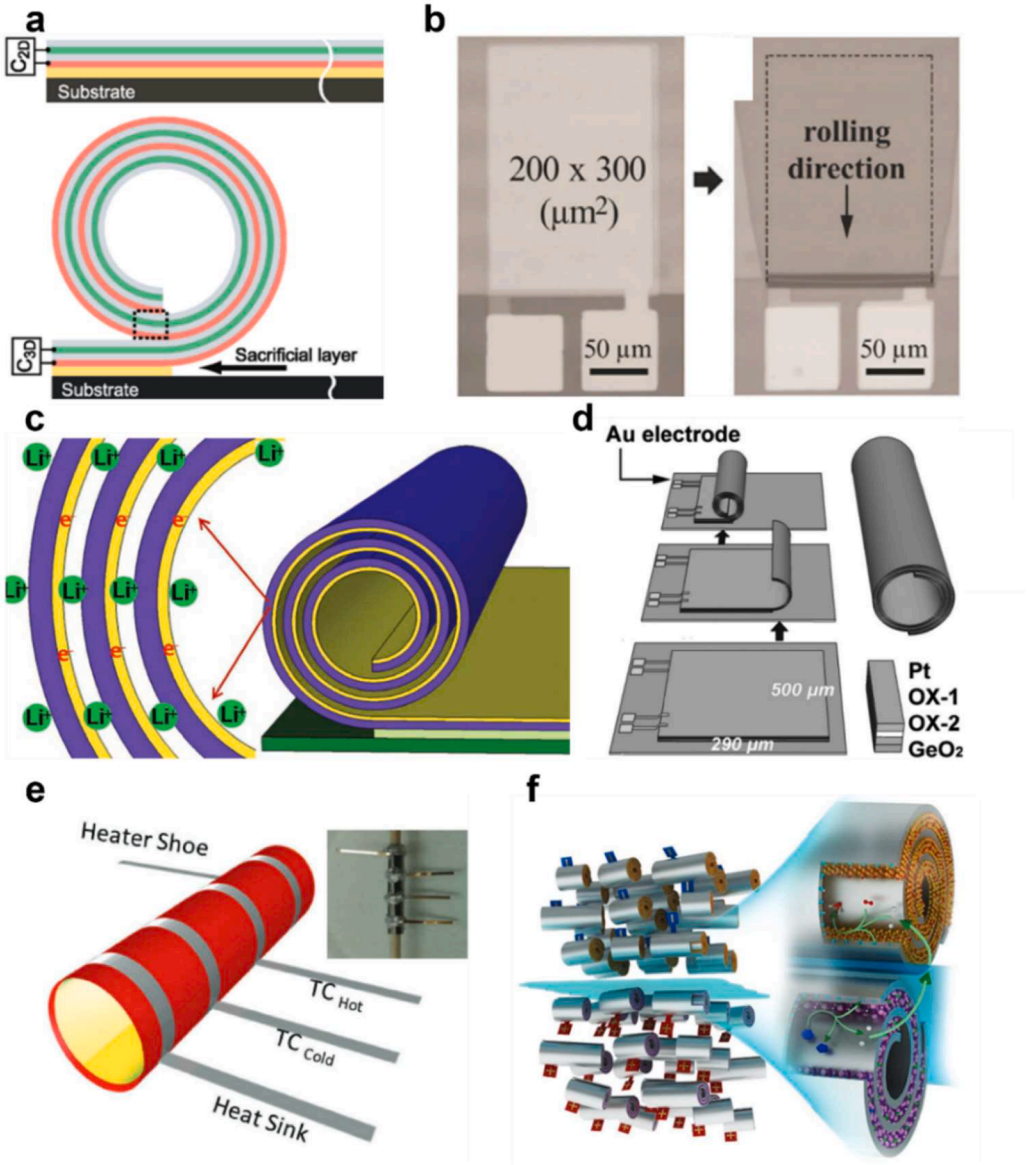

Fig. 7. Rolled-up microenergy devices. a, Layer sequence of rolled-up energy storage capacitor. b, Optical microscopy images of rolled-up electrostatic energy storage capacitor before and after rolling. c, Schematic illustration of the rolled-up lithium-ion storage microcell. d, Schematic diagram of the Pt-RuO_2 rolled-up microtubes. e, Schematic of rolled-up thermoelectric generators. f, Schematic setup of rolled-up enzyme-driven glucose biofuel cells. Reproduced with permission. Copyright © 2010, American Chemical Society. Copyright © 2012, 2014, 2017, 2018 Wiley-VCH.

reading heads (Fig. 6c), widely employed in conventional magnetic storage technologies, are capable of detecting different magnetic domain orientations, while transverse pulsed currents are applied in magnetic domain writing operations (Fig. 6d, h). During the application of transverse pulsed currents, the intense local magnetic field generated by the transverse current switches the magnetization of adjacent domains, aligning their magnetic moments with the induced magnetic field. Furthermore, pulsed currents of opposing polarities generate induced magnetic fields in opposite directions, yielding distinct domain orientations and enabling the writing of specific data bits [133]. Regarding information readout, in addition to the traditional GMR reading head scheme, readout methods based on the anomalous Hall effect (AHE) have emerged as novel low-power, high-speed readout solutions. Magnetic materials with PMA exhibit the anomalous Hall effect when subjected to a longitudinal current, resulting in distinct transverse potential differences corresponding to specific domain orientations. Consequently, low-power readout capabilities can be realized through circuit designs that measure this transverse anomalous Hall voltage [134].

In contrast to conventional magnetic disk storage, domain wall memory circumvents the limitations associated with mechanical rotation; domain walls and magnetic domains can move at high velocities, enabling ultra-fast read and write operations for magnetic storage [136]. Furthermore, by selecting appropriate magnetic functional layers, the threshold current required to drive domain wall motion can be reduced to relatively low magnitudes, resulting in minimal power consumption during operation [136]. Overall, owing to their superior storage performance, domain wall memory devices have emerged as a focal point within the field of spintronic device research. However, the on-chip storage density of these devices remains constrained by the 2D planar geometry. Consequently, research efforts have increasingly shifted toward the development of 3D structural configurations for memory devices (Fig. 6a, e). In 2022, researchers proposed a method to realize 3D domain wall memory devices by fabricating 3D microstructures on an alumina surface (Fig. 6f) and subsequently transferring the memory devices onto these structures via a MEMS thin-film transfer process

[135] (Fig. 6g). While this approach enhances on-chip information storage density, the resulting 3D microarchitectures exhibit a degree of randomness, leading to a lack of controllability in device performance. Moreover, the transfer process is incompatible with CMOS technology, rendering large-scale fabrication difficult. To further advance the realization of 3D domain wall storage, in 2024, researchers introduced a 3D rolled-up domain wall memory technology (Fig. 6i, j) based on polyimide hydrogels [133]. This method employed a rolling mechanism facilitated by wet etching and liquid-phase-assisted hydrogel swelling to fabricate 3D rolled-up devices. By transforming planar domain wall memory devices into 3D rolled-up structures, this approach significantly reduced the on-chip footprint and increased information storage density. This technique is compatible with CMOS processes and enables the stable fabrication of memory devices, thereby demonstrating the advantages and potential of rolled-up architectures in memory applications. Nevertheless, the rolling driving layer employed in this method consists of organic materials; to achieve more stable device performance, the development of rolled-up devices based on inorganic systems remains necessary. Furthermore, current magnetic materials still require relatively high driving currents (Fig. 6k), which generate substantial heat within the 3D rolled-up system and significantly impair device performance. Consequently, to attain superior device performance, further research and development are required in areas such as packaging technologies with high heat dissipation capacity and mechanical strength, as well as high-performance magnetic materials exhibiting low driving currents [133].

6. Rolled-up microenergy devices

Device miniaturization and integration have long constituted the primary developmental trajectory for IC devices. To power an increasing number of circuit components within lightweight and mobile systems, the development of miniaturized and integrated energy storage devices is being accelerated. Notably, micro-supercapacitors and microbatteries have demonstrated significant technological potential through extensive research. To achieve higher energy storage densities, 3D rolled-up architectures can be effectively integrated with capacitors and batteries, thereby attaining superior energy storage capabilities within a reduced on-chip footprint. The exceptional energy storage performance exhibited by these 3D rolled-up architectures underscores the application potential of this 3D strategy in micro-supercapacitors and microbatteries, offering a novel technological avenue for high-density, high-performance energy storage devices.

6.1. Rolled-up micro-supercapacitors

The rapid advancement in the integration density of micro- and nano-electronic systems has precipitated an urgent demand for miniaturized and integrated power sources [141], thereby driving the development of miniaturized energy storage devices and associated fabrication protocols. As primary components for miniaturized energy storage, capacitors have garnered considerable attention regarding their device architectures and fabrication strategies. For 2D energy storage capacitors-such as those utilizing 2D stacked, planar interdigitated, or other planar geometries-the enhancement of energy density is significantly impeded under volume-constrained conditions. To surmount this bottleneck, 3D rolled-up capacitors based on thin-film rolled-up technology were proposed and demonstrated [142] (Fig. 7a, b). These capacitors exhibited a footprint reduction of nearly two orders of magnitude compared to planar structures, achieving a capacitance density of approximately 200 $\mu F/cm^2$ and a specific energy of roughly 0.55 Wh/kg, thus serving as ultra-compact supercapacitors. Subsequently, researchers fabricated multi-turn rolled-up structures based on metal/dielectric stacks (e.g., $Al_2O_3/HfO_2/TiO_2$) [143], realizing the parallel fabrication of 1600 rolled-up capacitors on a 4-inch silicon wafer. The rolled-up capacitors demonstrated a 20-fold reduction in footprint compared to planar devices, while the multi-turn architecture doubled the capacitance value. These findings validate the potential of 3D rolled-up capacitors for scalable batch fabrication and ultra-high energy density applications.

6.2. Rolled-up microbatteries

Micro-scale batteries capable of generating energy within micro- and nano-systems constitute a vital component complementary to energy storage systems. Despite the remarkable achievements realized in macro-scale battery technology, the fabrication of 3D batteries at the micro- and nano-scale remains a significant challenge [144]. 3D thin-film rolled-up technology enables the transformation of 2D films into rolled-up architectures, offering advantages such as high specific surface-to-volume ratios and shortened ion diffusion paths, alongside facile integration into electronic circuits. Consequently, this technology has been extensively investigated across various domains, including electrochemical batteries, fuel cells, thermoelectric generators, and biofuel cells. Researchers have proposed and designed 3D rolled-up lithium-ion batteries (Fig. 7c) based on multilayer nanomembranes composed of amorphous Ge and highly conductive Ti [145]. In this configuration, the Ti layer functions as an electron transport channel while simultaneously providing mechanical support for the Ge layer. The device exhibited an initial reversible capacity of 1495 mAh/g (at C/16), retaining approximately 930 mAh/g after 100 cycles-a substantial improvement in retention compared to pure Ge microtubes (≈600 mAh/g). Subsequently, researchers fabricated 3D rolled-up direct methanol fuel cells [146] by rolling RuO_2 thin films coated with Pt nanoparticles into tubular structures (Fig. 7d) and embedding them within a microfluidic channel. This fuel cell featured a footprint of 1.5×10^{-4} cm^2 and achieved a maximum power density of 257 mW/cm^2, representing an enhancement of three orders of magnitude compared to conventional micro-scale methanol fuel cells, alongside significantly improved stability. Beyond high-energy-density chemical batteries, 3D rolled-up technology can also be employed to fabricate thermoelectric converters. Researchers have demonstrated a 3D rolled-up micro--thermoelectric generator based on telluride thermoelectric thin films [147] (Fig. 7e). This tubular thermopile architecture facilitates the maintenance of a substantial temperature gradient, thereby enhancing power generation efficiency. Moreover, compared to conventional devices, it offers superior lightweight characteristics and higher material utilization efficiency. The fabricated Sb_2Te_3- and Bi_2Te_3-based 3D rolled-up thermoelectric generators produced a power output of 5 μW from 8 p-n junction pairs under a temperature difference of 60 °C. These results provide novel insights for micro-scale thermoelectric power generation applications and demonstrate the immense potential of 3D rolled-up architectures in physical field conversion. Furthermore, glucose biofuel cells based on bilayer rolled-up enzymatic nanomembranes (Fig. 7f) were successfully fabricated utilizing a similar process [148]. By immobilizing glucose dehydrogenase, diaphorase, and bilirubin oxidase within titanium nanomembranes, these devices demonstrated advantages such as high-power density and ultra-long discharge durations. The battery exhibited a maximum areal power density of approximately 3.7 mW/cm^2, a stable power output of roughly 0.8 mW/cm^2, and a continuous discharge time of up to 452 h, thereby offering a viable solution for powering implantable biomedical devices.

7. Conclusion

In this review, we have summarized the fabrication methods and recent progress in transforming planar designs into 3D tubular architecture. Rolled-up nanotechnology offers a versatile and facile approach for fabricating tubular structures with well-defined geometries. Recent advancements in rolled-up functional devices have expanded their applications across a variety of fields, including passive elements, FET sensors, photodetectors, magnetic sensors, domain wall memories and

Table 2
A comprehensive comparison of representative rolled-up on-chip devices.

Device (section)	Material	Fabrication	Structural design	Device-level metrics	Bottlenecks	Refs.
RF capacitors (Sec. 3.1)	Metal-dielectric-metal (MIM), Metal interdigital electrode	Sacrificial release (wet/dry), stress-gradient control; overlap definition	Tube diameter; turn number; electrode overlap length; interlayer spacing	>15 × *C* increase; ~371 pF/mm^2; equivalent lumped model includes parasitics	Incomplete high-frequency parasitic modeling	[90,91]
Inductors / magnetic inductors (Sec. 3.2)	Cu coil + magnetic core options (fluid core; laminated magnetic films)	Stress-driven rolling; post-electroplating thick Cu; integrated magnetic layers	Coil length/width; turns; spacing; tube elevation from substrate; core fill factor	L up to 1.24 μH@10 kHz; inductance density up to 8333 nH/mm^2@0.55 GHz; wafer-level yield ~92%	Thin metal due to limited rolling stress	[101,102, 39,48]
Transformers / LC resonators (Sec. 3.2)	Nested rolled coils; LC integration	Alignment of multi-layer coils; control of rolling direction; integration with capacitors	Coil nesting geometry; inter-winding dielectric; turn ratio; tube diameter	Coupling coefficient up to 0.95; ~90% area reduction; LC resonator ~10 × area reduction	Limited mmWave EM predictability	[40,41]
Integrated FET microtubes (sensing + microfluidics) (Sec. 4.1)	InGaAs/GaAs; IGZO; organic (CuPc); graphene	CMOS-compatible release; integration of circuits before rolling	Tube diameter; channel placement around circumference	Switch ratio >10^5; SS ~160 mV/dec; IGZO system-level circuits; r-OTFT <2 V	Reliability under cyclic bending and interfaces	[37,78,50, 125]
Rolled-up photodetectors (Sec. 4.2)	Te thermophotovoltaic; graphene-readout Si tube	Epitaxial and thin film transfer; control of cavity/absorption path	Tube cavity (diameter/length); optical coupling; incident-angle acceptance	Te TTD: responsivity 252.13 V/W; detectivity 1.48 × 10^{11} Jones; graphene-readout Si: 6803 A/W, 75 ns, 778 Mbps	Lack of transferable optical rules and heating	[43,129]
Magnetoresistance sensors (Sec. 4.3)	Co/Cu Py/Cu GMR (and related stacks) on stress-driving layer	Deposition stack control; stress/curvature tuning	Tube curvature; thickness of magnetic film; stacking sequence	Rolled-up device MR 20% improvement; 3D geometry enables vector sensing concepts	Limited sensitivity of direction detection; high power consumption	[37,123, 124,130]
Tubular magnetic domains / spin textures (Sec. 5.1)	Curvature/stress-tailored magnetic multilayers (e.g., Py, Ni etc.)	Controlled rolling radius; stacking structure; categories of magnetic materials	Diameter; winding; intermediate insulating interlayers	Tubular geometry enables new domain states	Unclear domain configurations of additional materials	[137,138, 140]
Rolled-up domain-wall (racetrack) memory (Sec. 5.2)	Magnetic DW devices; magnetic multilayers (e.g., CoFeB/Pt etc.)	Direct rolling; drive-current reduction	Racetrack length in tube; racetrack configuration	Higher on-chip storage density; Joule heating affects magnetic domain motion	High threshold current; heat accumulation	[133,135, 136]
Rolled-up energy-storage capacitors (Sec. 6.1)	Metal/dielectric stacks (e.g., $Al_2O_3/HfO_2/TiO_2$)	Parallel batch fabrication; dielectric stack deposition quality; release uniformity	Multi-turn architecture; footprint, turns; dielectric thickness	Footprint 2 orders decrease; storage density: 200 μF/cm^2, 0.55 Wh/kg; 1600 devices on 4-inch wafer;	Dielectric reliability; breakdown statistics	[142,143]
Microbatteries / fuel cells / thermoelectric / biofuel (Sec. 6.2)	Microcell (e.g., Ge/Ti-Li, Pt-RuO_2-methanol etc.); Sb_2Te_3/Bi_2Te_3 thermopile	Multilayer nanomembranes; catalyst coating; integration into microfluidic channel	Microfluidic channel; surface-to-volume ratio; thermal gradient path	Ge/Ti: 1495 mAh/g initial; fuel cell: 257 mW/cm^2; biofuel: max 3.7 mW/cm^2, discharge up to 452 h	Packaging; electrolyte compatibility, bio-stability	[145–148]

energy storage. To better clarify the relationships between materials, fabrication routes, structural design, the resulting physical properties, and device-level performance, Table 2 summarizes a comprehensive comparison of the representative rolled-up device families discussed in Sections 3-6. The table highlights the key design and process levers that shape tubular architectures, links them to the dominant property bottlenecks and performance metrics across different application domains. Despite the substantial challenges involved in material and process optimization and structural design (shown in Table 2), rolled-up technology retains excellent compatibility with standard CMOS technology. In addition, the definitive advantage of the 3D tubular architecture lies in its ability to bridge 2D planar patterns and 3D spatial structures via controllable self-rolling mechanisms, which enables enhanced magnetic coupling and optical coupling, unique spintronic phenomenon and high energy density. Owing to these distinct merits, thin-film self-rolling technology holds tremendous potential for the advancement of on-chip devices.

While the remarkable advancements in rolled-up nanotechnology, several technical hurdles must be overcome to fully unlock the potential of on-chip devices based on these platforms. One major challenge lies in severe ohmic losses. Typically, the strained layer needs to provide sufficient mechanical impetus for self-rolling. However, the presence of a functional layer clearly exerts a detrimental effect on this process, which inevitably compels the functional layer to be thinner than those found in traditional planar devices. One strategy to address this challenge is to optimize the strained layer, for instance, by tuning process parameters to enhance internal stress or by substituting it with high-stress material systems. Another effective method is the implementation of post-deposition techniques, such as chemical plating or electroplating to thicken the metal layer to a thickness of tens of micrometers [149,150].

Secondly, heat accumulation represents a significant challenge for 3D tubular devices. Specifically, due to the detachment of the device body of tubular devices from the substrate, joule heat is limited to dissipation through the air, lacking the direct thermal path to the substrate available to planar devices, resulting in performance degradation and reliability degradation of on-chip devices. One effective strategy to address this issue is incorporating a dedicated thermally conductive layer, such as AlN, h-BN, or DLC, into the thin-film stack [151–154]. Alternatively, the tubular structure can be leveraged as a microfluidic channel to circulate coolant for active heat dissipation. Specifically, the liquid flowing through these tubular structures dissipates the heat generated by the device, thereby preventing overheating.

Thirdly, whether for discrete components or integrated circuits, the practical application of 3D tubular devices necessitates the development of novel 3D packaging technologies. Such technologies are essential to prevent deformation from external mechanical forces and ensure long-

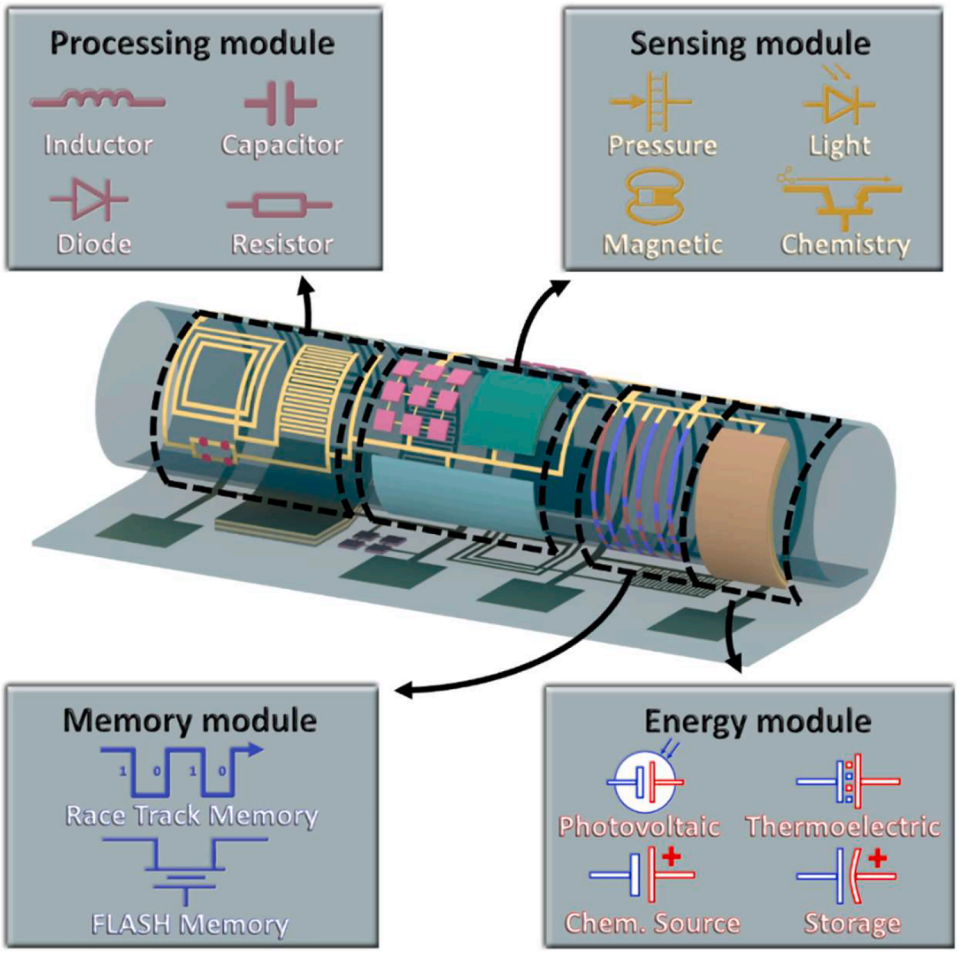

Fig. 8. Fully functional 3D rolled-up circuits. Conceptual schematic of a multifunctional tubular electronic system formed by strain-driven self-rolling, enabling heterogeneous components to be co-integrated along the tube circumference and axis. Representative modules include a processing module (inductor, capacitor, diode, resistor), a sensing module (pressure, light, magnetic, and chemical sensing), a memory module (rolled-up racetrack memory and flash memory), and an energy module (photovoltaic, thermoelectric, chemical energy sources, and on-board storage).

term stability in ambient environments. A quasi-static volume dispensing process coated with a thick layer of polymer (SU-8) has been successfully implemented in tubular devices to achieve good encapsulation [155]. Depositing a conformal Al_2O_3 layer via ALD is another effective strategy to enhance the mechanical structural robustness of 3D tubular devices. Currently, these packaging techniques are not yet fully developed, largely because they narrowly focus on mechanical reinforcement. In the context of on-chip devices, however, it is equally crucial to address thermal management and electromagnetic interference (EMI) shielding.

Building on the device demonstrations summarized in Table 2, several research directions stand out as particularly impactful:

Materials and nanomembranes stack co-optimization for efficient, high-drive rolling: A recurring trade-off is the tension between strong rolling drive and low electrical/thermal loss. Future work should focus on stack designs and materials that jointly optimize stress engineering, conductivity, dielectric/magnetic loss, and interface integrity, combined with robust post-processing (e.g., plating) that improves electrical performance without sacrificing geometric controllability.

1) System-level heterogeneous integration toward "rolled-up circuits": a promising avenue for future research lies in integrating various rolled-up components into a unified tubular structure, thereby forming fully functional 3D rolled-up circuits (Figure 8). Realizing the vision in Figure 8 requires advances in interconnect routing, modular assembly, and testing strategies specifically for tubular platforms. Hybrid integration-combining rolled-up architectures with emerging systems (e.g., 2D materials) via transfer methods-offers a practical path to multifunctionality. This approach avoids the complexity and constraints of optimizing a single monolithic stack.
2) Reliability-first engineering: packaging, drift, and lifetime benchmarking. As rolled-up devices transition from proof-of-concept to practical modules, reliability must be prioritized alongside peak performance. Key opportunities include developing conformal barriers, geometry-compatible sealing, and packaging with thermal management. Furthermore, consistent benchmarking of drift and lifetime under electrical, thermal, and mechanical stress is essential.

CRediT authorship contribution statement

Li Chen: Writing – review & editing, Writing – original draft. **Yuhang Chi:** Writing – review & editing. **Shengbao Liu:** Writing – review & editing. **Gaoshan Huang:** Writing – review & editing. **Yongfeng Mei:** Writing – review & editing. **Jizhai Cui:** Writing – review & editing, Supervision, Resources, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Supplementary materials

Supplementary material associated with this article can be found, in the online version, at doi:10.1016/j.mtelec.2026.100213.

Data availability

No data was used for the research described in the article.

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