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Thickness-Dependent Electronic Transport in Ultrathin, Single Crystalline Silicon Nanomembranes

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As distinct from bulk silicon, ultrathin silicon-on-insulator (SOI) or silicon nanomembranes (Si-NMs) offer excellent electronic and mechanical properties that are essential to the development of electronic/optoelectronic systems. Ultrathin Si-NM field effect transistors (FETs) based on p-doped SOI (100) wafers are investigated. The thickness of the Si-NMs is controllably reduced from 50 nm to 10 nm through the use of a unique etching process. Based on systematic investigation of Si-NM FETs with varying thicknesses, both insulating and metallic behaviors are observed, which can be attributed to carrier enhancement by surface-dipole doping after thickness reduction. Spectroscopy characterization and theoretical simulations reveal that this high surface-dipole density can be inverted, yielding high-density electrons regardless of the bulk p-doped nature of the material, thus significantly enhancing its conductivity. These findings offer a physical understanding of thickness dependence, which is critical to the future development of ultrathin SOI electronics, of relevance to a diverse range of semiconductor applications.

1. Introduction

Ultrathin silicon-on-insulator (SOI), referring to a structure of silicon nanomembranes (Si-NMs) on insulating substrates, offers attractive capabilities as electronic devices[1–5] for broad applications from thin film transistor to flexible electronic systems.[6–11] The SOI-based field effect transistors (FETs) are of great interest because they possess excellent advantages to overcome short channel effects for continuing size shrinking.[1,12] The Si-NM FETs built on ultrathin SOI, which possesses a large surface to volume ratio, are also highly sensitive to the surrounding environment such as surface chemical adsorbates.[13,14] Previous electronic transport studies of (001) SOI reveal an interaction between surface and bulk states,[15] which enhances the conductivity of the surface region in Si-NMs. Systematic studies on surface-reconstructed and hydrofluoric (HF)-treated Si-NMs also stress the significance of surface treatment on electrical transport properties of Si-NMs. For example, surface HF treatments well explored in p-doped SOI (001) pin the Fermi level close to the conduction band of Si-NMs, which leads to surface accumulation of electrons so that reducing the sheet resistance.[15] Experimental investigations on the influence of surface condition[16,17] have been conducted on various semiconductors, such as bulk silicon[18,19] and ZnO.[20] However, the ultrathin Si-NMs (down to the scale of 10 nm thick) have not been carefully studied yet. Therefore, it demands additional experimental investigations to achieve a more thorough understanding of surface carrier transport mechanism in ultrathin Si-NMs.

In this work, we exploit Si-NM FETs with various thicknesses. By varying the thickness of ultrathin Si-NMs (50, 30,

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.201900232.

DOI: 10.1002/aelm.201900232

20, and 10 nm), we observe a thickness-dependent conductivity variation and an apparent conductivity enhancement on 10 nm thick Si-NM FETs ($\sigma = 24.3\ \Omega^{-1}\ cm^{-1}$ at 10 K and $\sigma = 33.6\ \Omega^{-1}\ cm^{-1}$ at 300 K). Additional temperature-dependent conductivity measurement of Si-NMs confirms a transition from insulating states in 50 nm Si-NMs to metallic states in 10 nm Si-NMs. Such transition can be attributed to the modulation of carrier density by the surface dipole doping and thickness variation, where the surface dipoles result from surface electronegative groups (O—H) introduced by HF treatment. Systematic analysis of X-ray photoelectron spectroscopy (XPS), ultraviolet photoelectron spectroscopy (UPS), and the corresponding simulation results indicate that ultrathin Si-NMs can be inversed by surface dipoles, inducing high density of surface electrons regardless of its p-doped bulk property. These findings establish great potential applications of semiconductor nanomembrane devices.

2. Result and Discussion

2.1. Preparation of Si-NMs and Device Fabrication

The processing of the ultrathin Si-NM is based on commercial p-doped SOI (100) wafer with an initial 50 nm thick Si-NMs and a 120 nm thick buried oxide. An initial resistivity of 11.51 Ω cm was probed by four-point measurement (Jandel, RM3000 Test Unit), corresponding to a boron doping level of $\approx 10^{16}\ cm^{-3}$.[21] Then a controlled thickness-reduction process was conducted by oxidation under 90% ozone atmosphere at room temperature for 12 min, followed by wet etching to strip the oxidization layer using 10% HF solution for 90 s,[22] as shown in **Figure 1**A. Such oxidation-stripping cycle was repeated until the target thickness is achieved. A stable thickness removal rate was calculated as ≈1.3 nm per cycle. Thus, 26 cycles can reduce the initial 50 nm thick Si-NM to 10 nm thick Si-NM.

It has been reported that surface reconstruction occurs spontaneously on a clean semiconductor surface.[23] However, no apparent surface reconstruction is observed from our processed Si-NMs, as shown in a high-resolution transmission electron microscope (HR-TEM, Philips CM200FEG) image in Figure 1B. The inset shows the corresponding diffraction spectroscopy, indicative of an excellent single crystalline structure. The absence of surface reconstruction at room temperature indicates that the fresh surface of Si (100) is not terminated by dangling bonds, but decorated under the circumstance of HF treatment. An ultrathin Si-NM characterized by a TEM is shown in Figure 1C, confirming a successful thickness reduction to ≈10 nm that is typically much smaller than the bulk silicon depletion length.[24]

After the thickness reduction of Si-NM, standard device processing techniques enable fabrication of high-performance electronics on the SOI platforms. First, photolithography process defined the active region followed by a dry etching process. Cr/Au (5/50 nm) contact electrodes were then deposited by electron-beam evaporation, and a subsequent rapid thermal annealing was carried out at 500 °C in Ar atmosphere for 3 min to improve the electrical contact. The highly doped bulk silicon underneath the SiO_2 performed as a back gate. The schematic illustration of the Si-NM FET is shown in **Figure 2**A. The upper inset is an optical image of a Si-NM device (channel length L = 5 µm, width W = 10 µm). The as-fabricated devices were measured in a Lakeshore vacuum probe-station using semiconductor parameter analyzer (Keithley, SCS-4200).

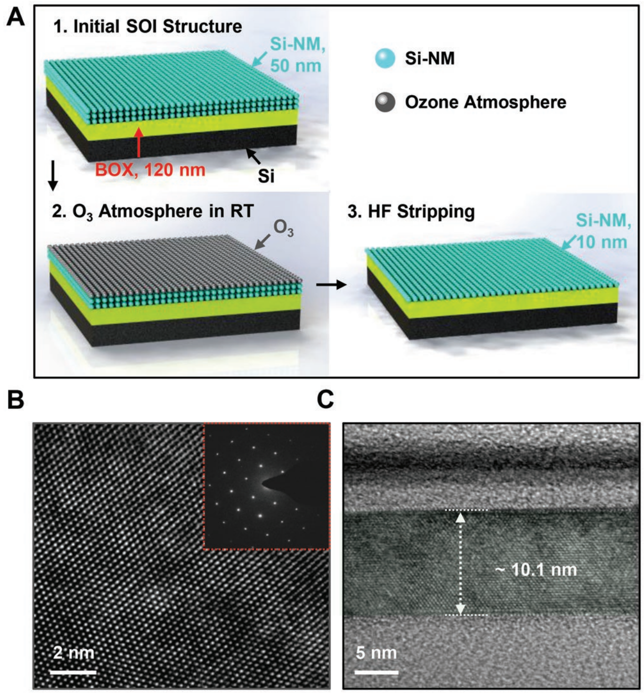

Figure 1. Ultrathin Si-NM reduction process and corresponding characteristics. A) Schematic of our HF treatment process: thermal oxidation under 90% ozone atmosphere for 12 min at room temperature and stripping the oxide using 10% HF solution for 90 s. After 26 cycles, the thickness of Si-NM sample can be thinned from 50 to 10 nm. B) SEM image of HF-thinned Si-NM. Inset is a low-energy-electron-diffraction image of HF-thinned Si-NM, indicative of little surface reconstruction. C) High-resolution TEM of a 10 nm thick Si-NM.

2.2. Basic Electronic Transport Measurement

A Schottky contact forms between lightly doped Si-NMs and the deposited metal (here Cr/Au). In an ideal scenario, Schottky–Mott rule[24] can be satisfied by

$$q\varnothing_b = W_m - \chi \tag{1}$$

where q is the electron charge and $\varnothing_b$ is the Schottky barrier height (SBH), W_m is metal's work function (WF), and χ is the electron affinity. Thus, the SBH here is given as 0.6 eV (χ of Si is 4.05 eV and W_m of Cr is 4.65 eV). Figure 2B displays a typical Schottky-type $|I_{DS}|$–V_{DS} characteristic for a 10 nm thick Si-NM FET under 1 V gate voltage (V_{GS}). The I_{DS} does not saturate under large V_{DS}, which can be attributed to the Schottky contacts at the metal-semiconductor interface and the surface-state effect. The former leads to carrier injection by thermionic emission across Schottky barrier that is tuned by gate voltage;[25] and the latter is related with the Si-NM thickness.[4,26] By applying large absolute values of V_{DS} to overcome the SBH, Figure 2C

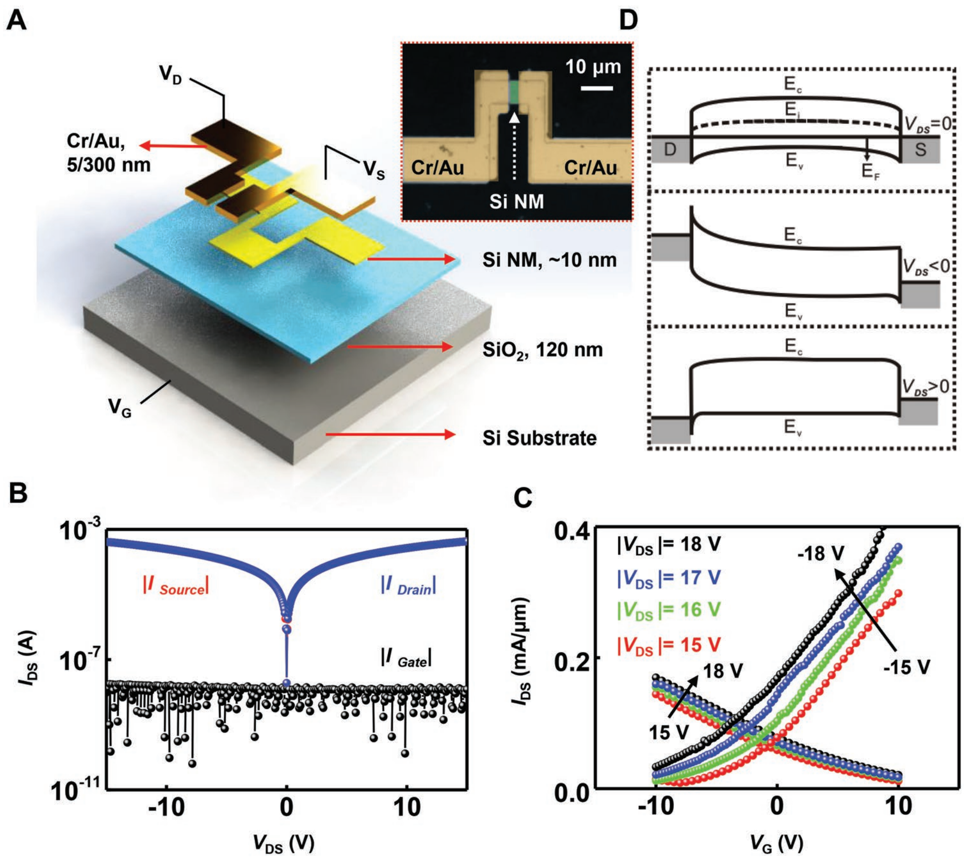

Figure 2. Basic electrical performance based on 10 nm thick Si-NM FETs. A) Schematic of the Si-NM FET structure. B) $|I_{DS}|$–V_{DS} curve at room temperature when V_G is fixed at 1 V in a 10 nm thick Si-NM FET. Gate leakage current is plotted by black dots. C) Transfer characteristics of the Si-NM FET. Along the direction of the arrows, V_{DS} changes by steps of 1 V. D) Band profiles of Si-NM FETs at various source-drain biases when V_{DS} = 0, <0, and >0.

displays the transfer characteristics of $|I_{DS}|$–V_{GS} curves measured under different V_{DS}. The corresponding band profiles with V_{DS} at 0 V (upper), a large negative value (middle), and a large positive bias (lower) are illustrated in Figure 2D. It should be noted that the transfer curves show only moderate gate control capability, which is consistent with previous report,[27] possibly due to several reasons: i) a low capacitance of back-gate using 120 nm thick low-k SiO_2 dielectric layer, ii) a strong interface scattering between Si-NMs and SiO_2, and iii) existence of surface states with a large surface-to-volume ratio that impedes the modulation of the Fermi level by gate control. All these can give rise to a low current on/off ratio. Thus, the above electrical measurement results strongly suggest that the surface states dominate electronic transport in our ultrathin Si-NMs.

2.3. Temperature-Dependent Electronic Transport Measurement

Figure 3A displays temperature-dependent I_{DS}–V_{DS} curves for a 10 nm thick Si-NM FET with V_G fixed at 0 V. From 10 to 300 K, I_{DS} first increases and then gradually decreases when temperature is higher than 180 K. This phenomenon is demonstrated more clearly in Figure 3B, where the channel conductivity σ versus temperature T is shown for various Si-NM thicknesses (10, 20, 30, and 50 nm). Based on a simple transport model, the temperature-dependent σ is mainly contributed by thermally activated electrons injected through the Schottky barrier

$$J = A^{*}T^{2}\exp\left(-\frac{q\varnothing_{b}}{kT}\right)\exp\left(\left(-\frac{qV_{DS}}{kT}\right)-1\right) \tag{2}$$

where T is the absolute temperature, A^* is the effective Richardson constant, q is electron charge, and k is the Boltzmann constant. Under this scheme, the temperature-dependent characteristics are mostly influenced by the Schottky barrier and regardless of carrier transport in the channel. For larger V_{DS}, tunneling current through Schottky barrier starts to dominate the carrier transport, which is implied by constant slopes in I_{DS}–V_{DS} curves. In the following analysis of electrical transport property, all data are measured at V_{DS} = 10 V. Using Wentzel–Kramers–Brillouin approximation, the tunneling current is given by[28]

$$J \propto \exp\left(-\frac{2W}{\hbar}\left(2m\left(\varnothing_{b}-E\right)\right)^{1/2}\right) \tag{3}$$

which is independent of temperature (where E is the electron energy, m is the electron mass, and W is the Schottky barrier width). That is to say, the effect of the Schottky barrier to the contact can be regarded as an additional "Ohmic resistance"

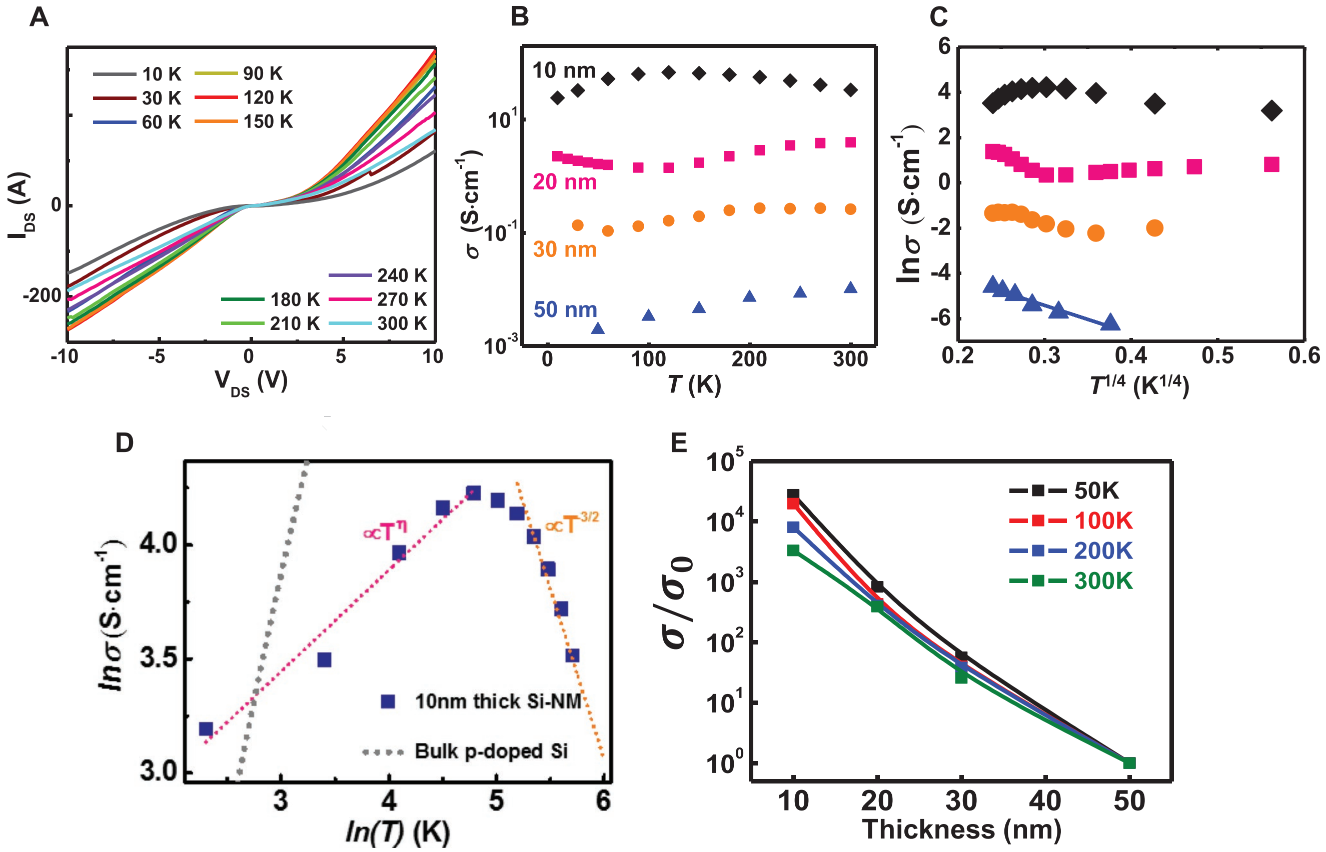

Figure 3. The temperature-dependent property and analysis of Si-NM FETs with various thickness. A) Temperature-dependent I_{DS}–V_{DS} measurement of a 10 nm thick Si-NM FET when gate voltage V_G is fixed at 0 V. B) Temperature-dependent conductivity of different thickness Si-NM. C) Re-plot of (B) using lnσ versus $T^{-1/4}$ coordinates, where blue line shows acceptable linear fitting of 50 nm Si-NM data and others show obvious deviation from linear relationship. D) Re-plotted temperature-dependent conductivity of 10 nm thick Si-NM with lnσ versus ln$T$ coordinate. Red and yellow dash line shows best linear fitting with $T^{-\eta}$, $\eta \approx 0.5$, and $T^{3/2}$, respectively. The gray dash line shows an increasing tendency of conductivity for bulk p-doped semiconductor. E) Conductivity as a function of thicknesses (300 K). The dots are experimental data and the dashed line is a fitting curve. σ_0 is the conductivity of 50 nm thick Si-NM at each temperature.

which maintains constant during temperature variation. Without applying V_{GS}, the fully depleted p-doped Si-NMs are expected to display an insulating state. In this regime, the electrical transport can be described as "hopping" of carriers between localized states via tunneling, where σ scales as[29]

$$\sigma(T) \propto \exp\left(-\left(T_0/T\right)^s\right) \tag{4}$$

where T_0 is a parameter related to the density of states (DOS) near Fermi energy and $s = 1/4$ corresponds to variable-range hopping.[30] Based on this model, the measured results from the 50 nm thick device (blue triangles) provide a perfect linear fitting from 10 to 300 K, showing an ideal insulating state. However, the results from thinner Si-NMs (30, 20, and 10 nm thick ones) show the increment of conductivity σ at low temperature and obvious deviation from linear fitting, which indicates different electrical transport mechanism in these samples (see more details in the Appendix and Figure S1, Supporting Information).

The 10 nm thick Si-NM FET has a relatively large σ in the whole temperature range, indicating a high carrier density. At low temperature, the conductivity variation mainly arises from CI scattering. In this regime, CI scattering in the p-doped silicon (gray dashed line in Figure 3D, see details in the Appendix, Supporting Information) usually follows

$$\ln\sigma_{\text{low}-T} = \frac{3}{2}\cdot\ln(T) - \frac{E_d}{2k_B}\cdot\exp(-\ln T) + \ln\sigma_0 \tag{5}$$

However, it cannot be applied in our case because of the screening effect from high carrier density. By including the screening effect, the experimental data can be fitted by the following equation from 10 to 120 K

$$\ln\sigma_{\text{low}-T} = \eta\cdot\ln(T) + \ln\sigma_0' \tag{6}$$

where $\eta \approx 1/2$ (red dashed line in Figure 3D), which indicates that long-range Coulomb potential is screened by electrons ($V^{\text{screen}}(r) \propto 1/R^2$, see details in the Appendix, Supporting Information). As temperature increases, CI scattering is further suppressed (scattering rate $w_{\text{im}} = \tau_{\text{im}}^{-1} \propto \langle v\rangle^2 \propto T^{-1/2}$) and acoustic phonon scattering starts to dominate. A degradation of σ is obvious when T is larger than 120 K, showing a phonon-limited transport that can be fitted by $\sigma_{\text{high}-T} \propto T^{-\frac{3}{2}}$ (plotted in Figure 3C by the yellow dashed line). Based on the above temperature-dependent measurement and the definition of metallic state (finite conductivity when $T \rightarrow 0$, and positive temperature coefficient of σ for metallic semiconductor[31]), we conclude that although not a typical metal, our 10 nm thick Si-NM is partially metallic.

In Figure 3E, the thickness dependence of σ is extracted from Figure 3B at 300 K, where σ_0 is the conductivity of 50 nm thick Si-NM at 300 K. Apparently the ratio of σ/σ_0 decreases with increasing thickness, thus the insulator-metal (I-M) transition possibly exists when reducing the thickness. Such transition is normally induced when carrier density increases above a critical concentration (n_{crit}) and satisfies the requirement: $a_b \cdot n_{crit}^{1/3} = 0.25$, where a_b is the effective Bohr radius of acceptor electrons.[32] The 20 nm and 30 nm thick Si-NMs appear to be near the transition point, as the carrier density is approaching critical concentration (n_{crit}). Such thickness dependence of σ is similar to that of ideal Si-NM (100) with surface π-band,[33] which is formed by surface reconstruction of dangling bond. However, in our experiment the surface of Si-NM is terminated by adsorbed molecules instead of dangling bonds, after the HF treatment.

Thus, we attribute such I-M transition to two factors: thickness effect and surface dipoles. When reducing thickness, the effect of surface states becomes more significant. For the 10 nm thick Si-NMs, the density of surface state at the Si–SiO_2 interface is typically $10^{10} - 10^{12}$ cm^{-2}eV^{-1},[31,32] which is much larger than the area acceptor density, e.g., 10^9 cm^{-2}. Thus, the density of surface states is large enough to deplete holes near the interface and form a built-in electrical field. It further leads to a surface band bending, which causes the increase of σ by the surface carrier accumulation or even inversion. Recently, the σ increment from surface dipole has been experimentally demonstrated.[17,34,35] These results report that, after HF treatment the Fermi level at Si-vacuum interface indeed shifts and even pinned near the conduction band minimum for a wide range of bulk doping levels, resulting in an inversion from the initially nominally p-type to an n-type template layer.[34] The surface inversion is expected to arise from electronegative surface groups (O—H) introduced by HF treatment, as these groups can be regarded as surface dipoles due to large electro-negativity difference between O and H.[35] When the surface of silicon bonds with these groups, it also leads to an effect of surface doping, which induces dipole electrical field and band bending.

2.4. Surface Analysis and Band Modeling

In order to obtain the evidence of surface dipoles, XPS and UPS analysis of Si-NMs with various thicknesses (12, 27, and 50 nm) are also conducted, as shown in **Figure 4**. For 12 and 50 nm Si-NMs, both samples are immersed in HF solution (49% concentration) for 30 s right before the subsequent measurements. For 27 nm Si-NMs, the samples with and without HF treatments are both prepared for further comparison.

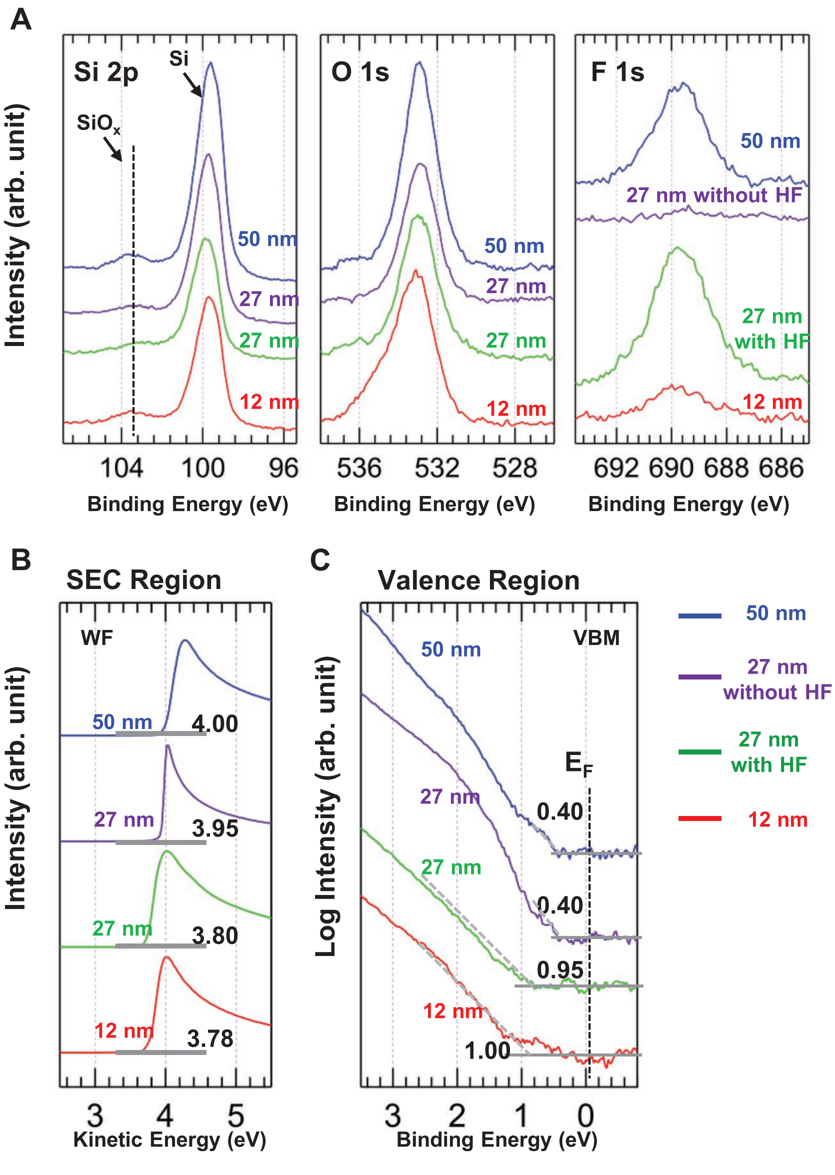

Figure 4. The XPS and UPS measurements of Si-NMs on SOI wafers with the various thicknesses. A) The XPS analysis of Si-NMs with different thickness level including 12, 27, and 50 nm, respectively. Each sample is completely immersed in HF solution (49% concentration) for 30 s right before the measurements except one of 27 nm thick Si-NMs (the purple lines). The XPS results display relative core peaks corresponding to different elements (Si 2p, O 1s, and F 1s). B,C) The UPS analysis of Si-NMs with various thicknesses in B) SEC and C) valence region, as a demonstration of the band structures. The SEC region shows the WFs and the valence region in log scale exhibits the VBMs of each thickness of Si-NMs. The corresponding zero binding energy (black dash line in C) in valence region refers to the Fermi level as an energy reference for all thickness measurements.

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The XPS spectral results of different samples, shown in Figure 4A, exhibit the element peaks of F 1s except for the 27 nm one without HF treatment, which confirms that the Si—F bonding is introduced during HF treatment. Besides, all samples show a detectable signal of (SiO_x) from the ultrathin native oxide layer (black dash line in Figure 4A, also consistent with results shown in Figure 1C). The hydrolysis reaction of Si—F bonding during the HF treatment also gives rise to extra Si—OH bonding as surface electronegative groups.[35] Therefore, the HF treatment to each thickness inevitably influences the doping of Si-NMs by the formation of surface dipoles.

Furthermore, Figure 4B,C exhibits the UPS measurements of Si-NMs with various thicknesses, showing the relative position of Fermi level. The secondary electron cutoff (SEC) region (Figure 4B) shows the shift of WFs with a clear trend, from 3.78 eV (12 nm) to 4.00 eV (50 nm). When the bandgap is expected to be constant, the Fermi level is gradually approaching the conduction band with decreasing thickness, which is an indication of stronger n-doping. Such an n-doping effect is thickness-dependent and correlated with the effective modulation of surface dipoles in thin Si-NMs. On the other hand, the valence band maximums (VBMs), which are defined by the energy difference between Fermi level and valence band edge, can be estimated at the valence edge (Figure 4C). The VBM increases from 0.4 to 1.0 eV with decreasing Si-NM thickness, indicating a higher n-doped state in thin Si-NM. For the 27 nm Si-NMs, VBM of the sample with HF treatment (0.95 eV) is apparently larger than that without HF treatment (0.4 eV), which confirms that HF treatment is critical to induce an n-doped state in thin Si-NM. Therefore, the ultrathin Si-NM can be inverted by surface dipoles from HF treatment regardless of its bulk p-doping nature, leading to an enhancement of carrier density and improved transport behavior, which is consistent with our electrical measurement results.

The band bending profile along the thickness direction (x-axis) of 50 nm thick Si-NM is schematically shown in **Figure 5**A. One position exists where built-in electric field and surface dipole electrical field are balanced, which is defined as boundary point. If surface dipole density is relatively low (trapped hole transport at Si–SiO_2 interfaces can be ignored), the conductivity of Si-NM mainly attributes to the electron transport in the inversion layer. However, for ultrathin Si-NMs (e.g., 10 nm thick Si-NM) or high surface dipole density, as shown in Figure 5B, surface dipole electrical field can go through the whole film. In this case, electrons flowing from source electrode can be accumulated in whole Si-NM and the surface state at the Si–SiO_2 interface will be filled by electrons. The total Si-NM is inverted from a normal p-type to an n-type with electron accumulation regardless of bulk doping property.

In order to quantitatively distinguish the influence between thickness and surface dipole, we conduct theoretical calculation. By solving Boltzmann–Poison equation numerically with an appropriate boundary condition, we found that changing thickness of Si-NM only leads to conductivity variation only within one magnitude, instead, this remarkable conductivity increasing tendency can be realized by enhancing surface dipole density from 10^{11} to 10^{13} cm^{-2}, which indicates that the increasing conductivity of thinner Si-NMs is mainly due to the enhancement of surface dipole density. The higher surface dipole density for thinner Si-NMs possibly results from the additional HF thinning cycles during the fabrication, as they can introduce more surface dipole absorption (for more details, see the Appendix, Figure S2, Supporting Information).

3. Conclusion

In summary, the repeated oxidation/wet-etching processing can effectively reduce Si-NM thickness to a controllable range approaching the quantum limit. A comprehensive investigation of experimental measurements and simulations was then explored based on such ultrathin Si-NM FETs. Temperature-dependent electronic transport of ultrathin SOI (100) displays an I-M transition in a range of varying thickness of Si-NMs (10, 20, 30, and 50 nm). We attribute this I-M transition to an enhancement of carrier density by higher surface dipole doping density absorbed during HF treatment. Corresponding

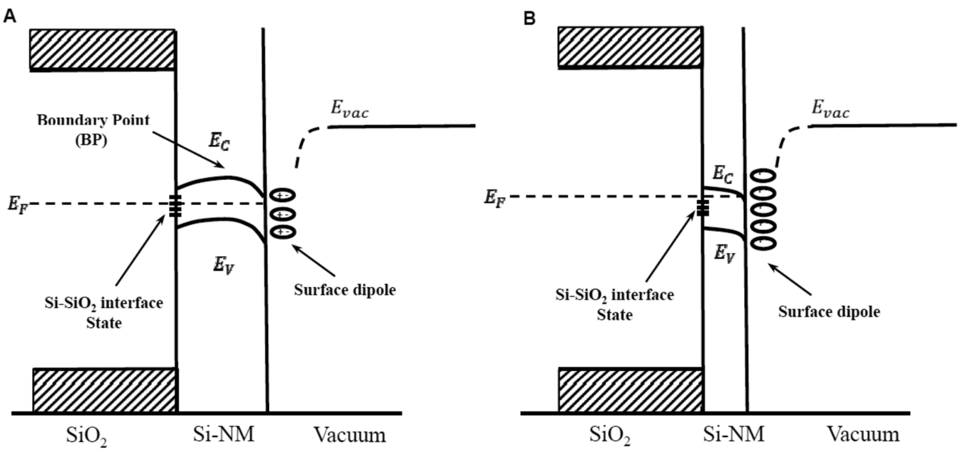

Figure 5. A comparison of band alignments between thicker Si-NM FETs (50 nm) and thinner Si-NM FETs (10 nm). A) Band bending profile for thick Si-NM (e.g., 50 nm thickness) with low surface dipole density. B) Band bending profile for thin Si-NM (e.g., 10 nm thickness) with high surface dipole density.

simulation results establish aspects of strong inversion that can be achieved on each thickness of Si-NMs with high surface dipole density (e.g., 10^{13} cm^{-2}), inducing high density of electrons regardless of its bulk p-doped property. A comprehensive combination of experiments and simulations highlights the enhancement of surface dipole density for ultrathin Si-NMs in temperature-dependent measurements that motivates more carriers and simultaneously improves conductivity. By modulating surface dipoles properly, ultrathin Si-NM-based FETs with unique characteristics have potential to become a new-generation platform for integrated electronic and optoelectronic systems.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

E.S. and Z.G. contributed equally to this work. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. This work was supported by the Natural Science Foundation of China (51322201, U1632115, 51602056), National Key Research and Development Program (2015ZX02102-003 and 2016YFA0203900), Science and Technology Commission of Shanghai Municipality (no. 17JC1401700), and the Changjiang Young Scholars Program of China. Part of the experimental work has been carried out in Fudan Nanofabrication Laboratory. References 22, 25, and 27 were updated on the 9th of July, 2019, after publication, as the author lists had been incorrectly reproduced.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

insulator-to-metal transition, silicon nanomembrane, surface dipole density, temperature dependence, ultrathin thickness

Received: March 2, 2019
Revised: April 4, 2019
Published online: May 12, 2019

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