NANO · MICRO small
www.small-journal.com

Flexible Transient Phototransistors by Use of Wafer-Compatible Transferred Silicon Nanomembranes

*Gongjin Li, Enming Song, Gaoshan Huang, Ruobing Pan, Qinglei Guo, Fei Ma, Bin Zhou, Zengfeng Di, and YongFeng Mei**

Flexible transient photodetectors, a form of optoelectronic sensors that can be physically self-destroyed in a controllable manner, could be one of the important components for future transient electronic systems. In this work, a scalable, device-first, and bottom-up thinning process enables the fabrication of a flexible transient phototransistor on a wafer-compatible transferred silicon nanomembrane. A gate modulation significantly restrains the dark current to 10^{-12} A. With full exposure of the light-sensitive channel, such a device yields an ultrahigh photo-to-dark current ratio of 10^7 with a responsivity of 1.34 A W^{-1} ($\lambda = 405$ nm). The use of a high-temperature degradable polymer transient interlayer realizes on-demand self-destruction of the fabricated phototransistors, which offers a solution to the technical security issue of advanced flexible electronics. Such demonstration paves a new way for designing transient optoelectronic devices with a wafer-compatible process.

1. Introduction

High-performance flexible electronics significantly expand the application of electronics in the Internet of Things era.[1–4] As an important component, a photodetector is the essential device for most optoelectronics due to its ability to convert light illumination into electrical signals.[5,6] Among the materials for a flexible photodetector, a single-crystalline silicon nanomembrane (Si-NM) attracts great attention due to its advances of mechanical bendability, optoelectronic sensitivity, and compatibility to current complementary metal oxide semiconductor technology.[7–11] The commonly known fabrication technique for a Si-NM photodetector is to release the Si-NM by removing the buried oxide layer of silicon-on-insulator (SOI) substrate and transferring it to the desired substrate via a wet or dry approach.[12,13] The main advantages of this approach include its simplicity, low-cost, and capability adapting to irregular surfaces.[14] However, the employment of aggressive etchants, incompatible to a high-temperature process, and difficulty in transferring large area continues Si-NMs often block their further applications.[15]

On the other hand, technical security is a common issue faced to all advanced electronics: their sensitive part should be remotely destroyed to avoid information leakage.[16] Recently, the transferable Si-NMs enable the realization of such transient devices.[17] Their ability to be physically or functionally self-destroyed in a controllable manner gives an ultimate solution to the security risk.[18] Traditionally, the transient functionality relies on the chemical dissolution of the active components of the devices.[19,20] Such a wet process exhibits unique convenience for implantable electronics since the devices could be destroyed in biological fluids.[21] Alternatively, the newly developed dry transient process is more suitable for non-bioapplications due to the higher reliability and better controllability of the transient process.[22–24]

Here, we designed and fabricated a flexible transient photodetector with metal-oxide-semiconductor field effect transistor (MOSFET) structure on a wafer-compatible transferred Si-NM. In the device construction, the Si-NM phototransistor was

G. J. Li, Prof. G. S. Huang, R. B. Pan, Dr. Q. L. Guo, F. Ma, Prof. Y. F. Mei
Department of Materials Science and State Key Laboratory of ASIC and Systems
Fudan University
Shanghai 200433, P. R. China
E-mail: yfm@fudan.edu.cn
Dr. E. M. Song
Center for Bio-Integrated Electronics
Frederick Seitz Materials Research Laboratory
University of Illinois at Urbana Champaign
Northwestern University
Evanston, IL 60208, USA
Prof. B. Zhou
Shanghai Key Laboratory of Special Artificial Microstructure Materials and Technology
School of Physics Science and Engineering
Tongji University
Shanghai 200092, P. R. China
Prof. Z. F. Di
Shanghai Institute of Microsystem and Information Technology
Chinese Academy of Sciences
Shanghai 200050, P. R. China
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/smll.201802985.

DOI: 10.1002/smll.201802985

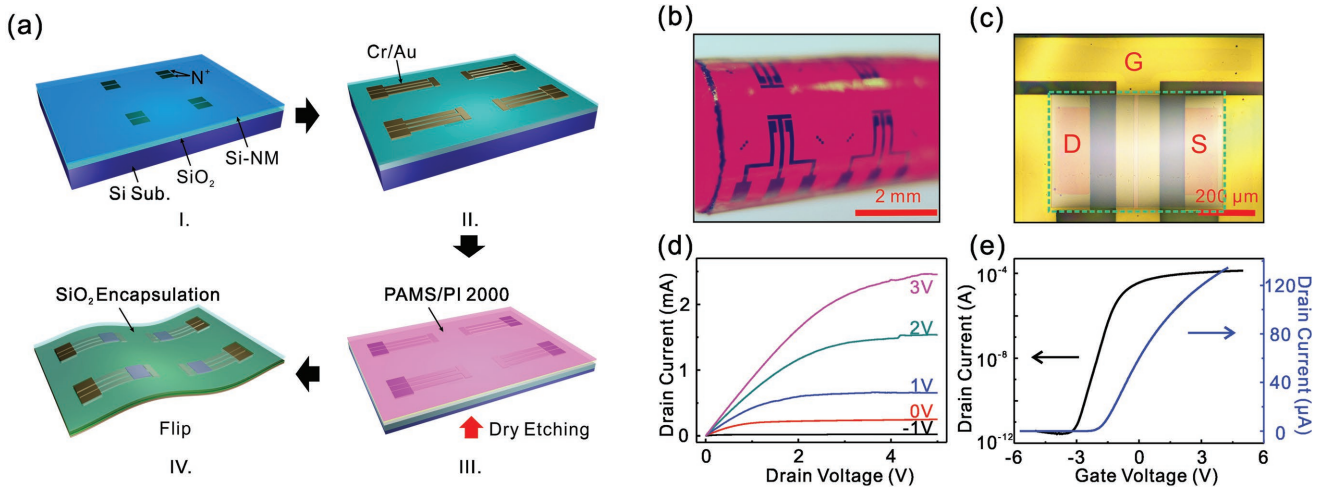

Figure 1. Fabrication process, morphology, and electronic properties of the Si-NM phototransistor. a) The scalable fabrication process: I. Forming source/drain n^+ regions with phosphorus doping. II. Device fabrication with a standard MOS process. III. Etching the back substrate with a dry etching process. IV. Releasing the flexible Si-NM phototransistor. b) A photograph of the Si-NM phototransistor array in the bending state. c) An optical microscope image of a Si-NM phototransistor. The green dashed rectangle labels the Si-NM area of the device. d) Output curves for device in dark with various gate voltages. e) Transfer curve for device in dark at a V_{DS} of 0.1 V.

prefabricated on SOI wafer directly by standard semiconductor technology and transferred after a bottom-up thinning process. All electrodes were arranged at the backside of the Si-NM phototransistor, which allowed full exposure of the light-sensitive channel to the illumination. Such a photodetector demonstrated a high optoelectronic responsivity due to the promoted photon-generated carrier separating efficiency.[25] In addition, a high-temperature degradable poly-α-methylstyrene (PAMS) interlayer was added below Si-NM to realize the transient functionality. At a temperature below PAMS degradation, the device operated stably and reliably. When triggered over its decomposition temperature (≈300 °C), nearly 100% PAMS degraded into the volatile products, leading to the destruction of the Si-NM phototransistor. The produced flexible transient phototransistor not only exhibited a series of excellent characters such as ultrahigh photo-to-dark current ratio, good linearity output, high gains, and tunable spectral responsibility, but also met the requirements to work functionally at a high-temperature environment.

2. Results and Discussion

2.1. Fabrication, Structure, and Electronic Properties of Si-NM Phototransistor

We designed a wafer-compatible process for high-performance Si-NM photodetectors with transient functionality. In order to investigate the optoelectronic response and the transient process, flexible Si-NM phototransistors were prepared through the fabrication steps demonstrated in **Figure 1**a. The detailed fabrication process is described in the Experimental Section and Figure S1 (Supporting Information). Briefly, a device-first strategy (labels I and II in Figure 1a) compatible to any high-temperature process in standard semiconductor technology is engaged to first produce the phototransistor on SOI substrate.[15] Then, a bottom-up thinning process (labels III and IV in Figure 1a) allows the transfer of Si-NM devices with size up to wafer scale to target flexible substrate (Kapton film in the present case).

The photograph in Figure 1b displays a Si-NM phototransistor array fabricated with the above-mentioned process. Nanomembrane devices array on a Kapton film in the bending state shows outstanding flexibility. Figure 1c presents an enlarged optical microscope image of an individual Si-NM phototransistor with the size of 400 × 600 μm^2, and the channel length (L) and width (W) of the device are 20 and 400 μm, respectively. The electrodes (D, drain; S, source; G, gate) are made by Cr/Au (5/100 nm) bi-layer. Figure 1d presents the output curves of the phototransistor at various gate bias voltages. The pinch-off point and saturation current increase with the gate voltage. Figure 1e exhibits the transfer characteristics in both semi-log and linear scale as a function of gate bias at a drain voltage (V_{DS}) of 0.1 V. The threshold voltage (V_T) is −1.8 V, estimated with a linear extrapolation method.[26] Such a negative threshold voltage is mainly due to defects in the SiO_2 gate dielectric deposited by a plasma-enhanced chemical vapor deposition (PECVD) process and can be further improved by increasing postmetallization anneal time or replacing the PECVD SiO_2 with thermal SiO_2.[27–29] The peak effective electron mobility is ≈410 cm^2 (V s)$^{-1}$, calculated from the slope of the transfer curve (Figure 1e) and output curve (Figure 1d).[30] More details about the electrical characterization (Figure S2, Supporting Information) and analysis of the device can be found in the Supporting Information. These gate controlled electronic performances are comparable with normal field-effect electronics on a bulk Si substrate.[31]

2.2. Optoelectronic Characteristics of the Si-NM Phototransistor

The gate modulation ability to the channel leads to remarkably enhanced light sensing ability of the fabricated phototransistor. **Figure 2**a exemplifies the optoelectronic response (I_{DS}, drain

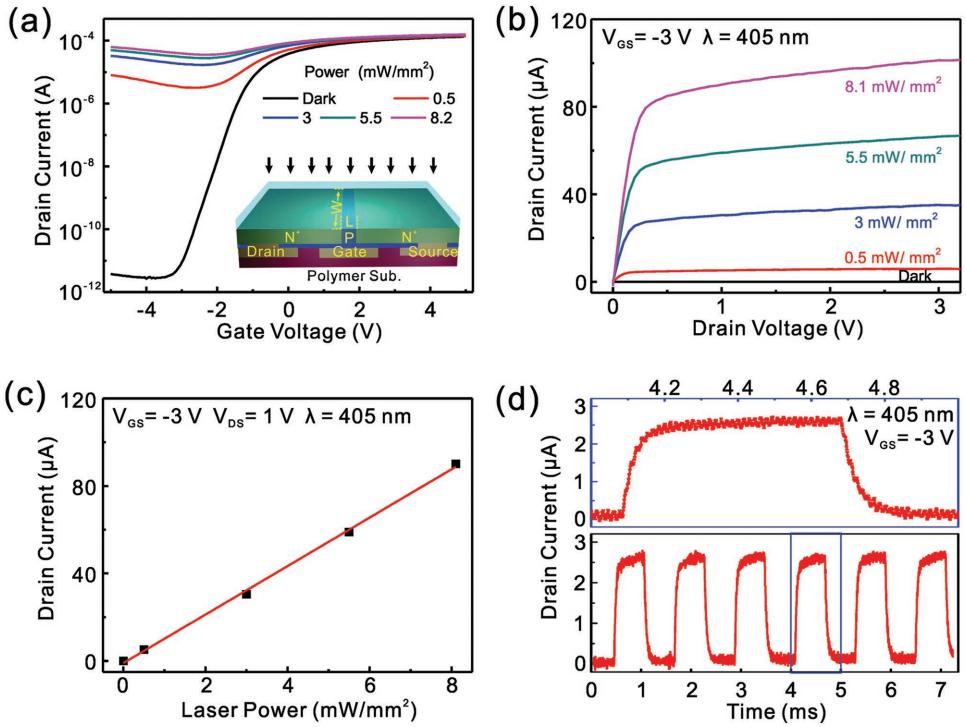

Figure 2. Optoelectronic properties of the Si-NM phototransistor. a) Drain current–gate voltage characterization under different irradiation intensity (405 nm) at a supply voltage (V_{DS}) of 0.1 V. Inset: A schematic illustration of the Si-NM phototransistor under illumination. b) Drain current–drain voltage characterization under different irradiation intensity (405 nm) at a gate voltage (V_{GS}) of −3 V. c) Linear response of the device. d) Response time characterization of the device at $V_{DS} = 1$ V and $V_{GS} = -3$ V. The illumination power is ≈0.3 mW mm^{-2}.

current) of the device with the gate voltage (V_{GS}) under different irradiation power (laser wavelength λ = 405 nm). The supply voltage (V_{DS}) is 0.1 V and the inset of Figure 2a schematically illustrates the cross-sectional view of the phototransistor. With all functionality stacks on the backside, the Si-NM interacts directly with irradiation. The I_{DS}–V_{GS} curves reveal that gate bias has a significant influence on the dark current of the phototransistor and limited impact to the photocurrent, which will be discussed later. One can see that in the range of $V_{GS} \geq 0$ V, the phototransistor is insensitive to illumination: the dark current and photocurrent are almost the same (≈10^{-4} A). While in the range of $V_{GS} < 0$ V, the dark current drops rapidly with the decrease of the gate voltage and becomes stable when $V_{GS} < -3$ V, and the phototransistor yields an ultrahigh photo-to-dark current ratio of ≈10^7 (varies with illumination intensity). To the best of our knowledge, this represents the highest photo-to-dark current ratio and excellent optical detectivity compared with previous reported Si-NM photodetectors.[32] Higher photo-to-dark current ratio brings larger distinction between photocurrent and dark current and therefore it is capable of detecting weak illumination. In brief, the phototransistor could operate with high photo-to-dark current ratio at negative gate bias and high current value at positive gate bias (see output curves with and without illumination in Figure S3 of the Supporting Information), which may cause higher responsibility at positive bias.

In order to further reveal the influence of voltage bias on the operation state of the phototransistor in the high photo-to-dark current ratio region, Figure 2b illustrates the I_{DS}–V_{DS} characteristics of the phototransistor at various illumination intensities ($V_{GS} = -3$ V), which reveals the influence of supply voltage (V_{DS}) on the optoelectronic response of the photodetector. At small V_{DS}, the photocurrent increases dramatically with the V_{DS} and then tends to be saturated at a higher voltage. Similar behaviors were also reported elsewhere,[33] as a higher V_{DS} allows an effective collection of photon-generated carriers during their lifetimes.[34] The dark current, on the contrary, remains sufficiently small even at higher V_{DS}. This character is useful to achieve high photo-to-dark current ratio. On the basis of these characterizations, the ideal working bias was set as $V_{GS} = -3$ V, $V_{DS} = 1$ V. Figure 2c exhibits the good linear response of the photocurrent as a function of the illumination power at this ideal condition. Here, the responsivity of the device (R_i) at λ = 405 nm irradiation can be estimated by

$$R_i = \frac{I}{P \cdot A} = 1.34 \text{ A/W} \quad (1)$$

where I is the photocurrent, P is the light power, and A is the active area of the phototransistor. The phototransistor could maintain such a good linear response even under weak illumination (Figure S4, Supporting Information). Figure 2d demonstrates the response speed of the photodetector. A semiconductor laser (λ = 405 nm, $P \approx 0.3$ mW mm^{-2}) equipped with an optical chopper serves as light source. A digital oscilloscope records the waveform. The responsibility of ≈1 A W^{-1} is similar to the value in steady state (see Equation (1)), indicating no output degradation in this high-speed switch mode. The phototransistor exhibits a rise (from 10% to 90% of peak

current value) and fall (from 90% to 10% of peak current value) time of 70 and 80 µs, respectively. These values are comparable to commercial phototransistors.[35]

The minimum detectable optical power (P_{min}) in the measurement bandwidth (DC to 1 kHz in the present experiment) can be estimated from the noise equivalent power (NEP)[36,37]

$$P_{min} = NEP = \frac{I_{noise}}{R_i} = 11.2\ \text{pW} \quad (2)$$

where I_{noise} is the output current in dark. Calculation shows that the P_{min} of our photodetector is lower than most of the reported silicon photodetectors.[38,39]

The upper panel of **Figure 3**a exhibits the experimental responsivity of the photodetector in the visible/near-infrared spectral range. The current Si-NM phototransistor exhibits an entirely different spectral response comparing with a commercial bulk silicon photodetector.[40] For bulk devices, the shallow penetration depth of short wavelength irradiation makes the photon-generated electron–hole pairs recombine largely on the surface before they are separated by an electric field, thus exhibits reduced responsibility.[41] For Si-NM devices with lateral structure in the present case, the surface contributes a lot to the carrier generation and transportation.[42] The spectral response drops obviously with the decrease of the absorption coefficient at long-wavelength range.[43] It is worth noting that the experimental spectral response in Figure 3a also exhibits several peaks at certain wavelengths. Previous research shows that, for certain irradiation wavelength and layer thickness, reflected light from interfaces enhances the total optical absorption in the active region.[44] Therefore, we established a simulation model to investigate the light propagation in our device with multilayered structure. The upper panel of Figure 3b schematically illustrates the trapping of incident light in Si-NM active layer sandwiched between SiO_2 encapsulation and metal electrode. The Au layer at the bottom prevents the penetration of irradiation wave and serves as a back reflector. The bottom panel of Figure 3b displays the electric field intensity in Si-NM at 405 nm. Here, all parameters are based on the actual layer thicknesses and optical data of the materials. Obviously, the multilayer structure concentrates the electric field in the Si-NM region. The calculated light absorption spectrum of Si-NM in the visible/near-infrared range is shown in the lower panel of Figure 3a. The absorption peaks in the simulated spectrum correspond well with those in the experimental result. The ultrahigh responsivity around 400 nm may benefit a lot from the wavelength-dependent light-trapping effect of the rough SiO_2 encapsulation layer.[45] It further proves that the interference between the interface reflections contributes to the responsivity enhancement at certain wavelengths. One may induce that the response of the photodetector could be tuned by changing the geometry of multilayered structure.

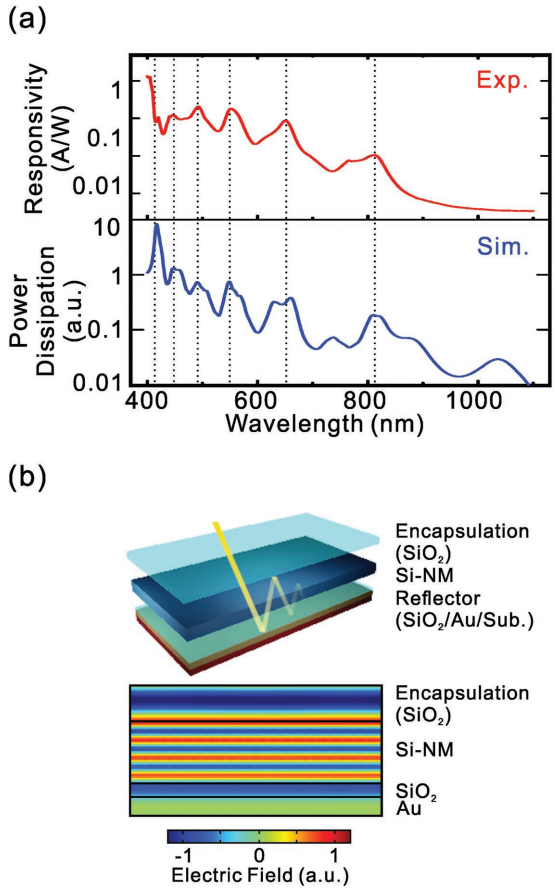

Figure 3. Spectral response and analysis. a) Experimental photocurrent spectrum (upper) and the simulated light power dissipation of the Si-NM layer (down). b) Schematic illustration of the optical path in the device (upper) and simulated electrical intensity distribution in the multilayer system of the device (down).

2.3. The Mechanism of Gate Bias Modulation

For high sensitive photoelectric detection, large dark current is not allowed. Structure features and gate modulation in our case thus conduce to the excellent detection characteristics of the phototransistor. The nanoscale thickness of Si-NM leads to thin channel in the phototransistor. A small conductive cross-section helps to reduce dark current. Although the nanoscale thickness makes the total absorption rather insufficient at a longer wavelength, average light absorbance per unit thickness in thin channel is still larger than thicker channel (bulk devices),[46] leading to the sensitive photodetection. In addition, both the metal electrode as a back reflector (Figure 3b) and the high carrier mobility in single crystal silicon nanomembranes enable the increase of on-state current.

Figure 4 reveals the mechanism of the gate modulation effect. The application of gate bias allows an effective control of energy band structure of the channel, as schematically shown in Figure 4a. Basic electronic characterization in Figure 1d,e indicates that the device behaves as a depletion mode n-channel MOSFET. The existence of positive charge in gate oxide reduces the barrier height at the source/drain contacts. In this case, the device has an appreciable channel conductance at zero gate voltage. Upper sketch in Figure 4a illustrates the corresponding energy band diagram. When a positive V_{DS} is applied on the drain contact, a noticeable amount of carriers transits through the channel, leading to a palpable dark current. In order to restrain the dark current, the energy band in channel needs to

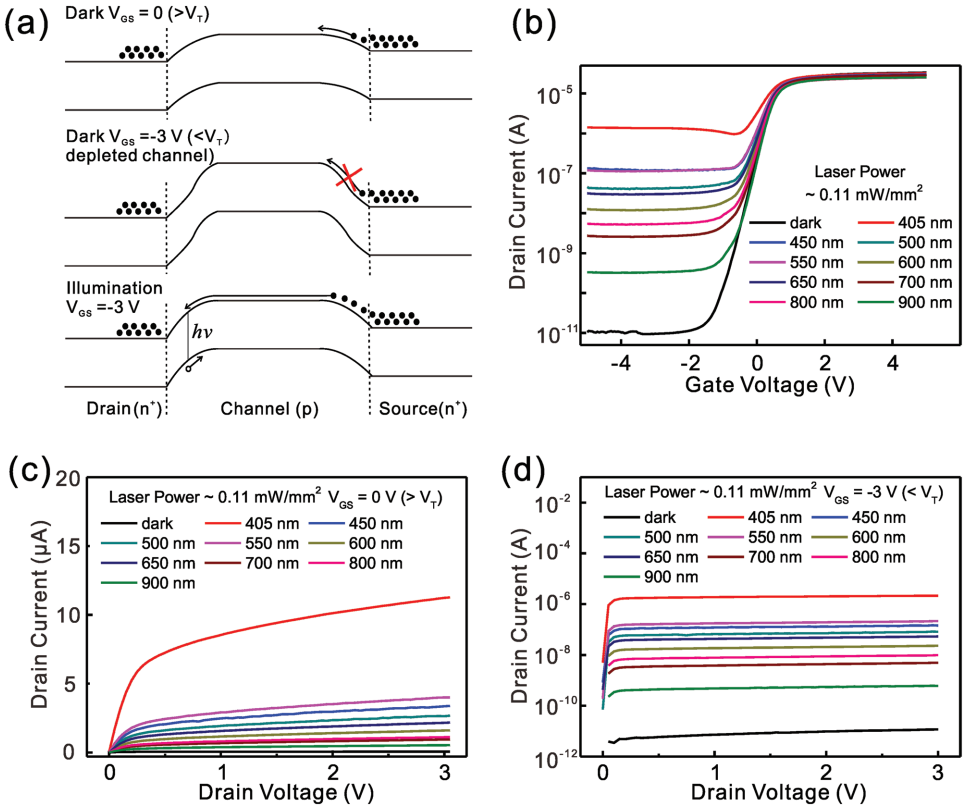

Figure 4. Mechanism analysis of the device. a) Energy band diagram of the phototransistor under different conditions. b) Tuning the operation mode with gate voltage under various illumination wavelengths. c) Output curves for the on-state mode of FET at various illumination wavelengths. d) Output curves for the off-state mode of FET at various illumination wavelengths.

be modified. Middle sketch in Figure 4a illustrates the increased barrier height by applying a negative gate bias. In the nanoscale thin channel, the applying of a negative gate bias (e.g., −3 V) depletes electrons in the channel.[47] The increased barrier height dramatically restrains dark current leakage through the device. When illuminated, the device exhibits a band diagram as shown in the lower sketch in Figure 4a. In this condition, the device behaves like a bipolar transistor.[48] Instead of providing base current, optically excited carriers in the channel can also trigger the transistor: when illuminated, the generated electrons diffuse into the positively biased drain region while the holes accumulate in the channel, leading to the decrease of barrier height.[49] Thus, electrons in source inject into the channel and result in large photocurrent. In addition, the use of single crystal silicon instead of amorphous one restrains the recombination of photon-generated carriers. The high aspect ratio (W/L = 20:1) of the device also helps to reduce channel length for sufficient channel area. These factors contribute to an efficient collection of photon-generated carriers during their lifetime. Briefly, the gate bias modulation plays a dominant role in the high photo-to-dark current ratio. The ultrathin Si-NM allows the depletion region throughout the whole channel under gate modulation. For a thicker channel (e.g., in bulk device), the field effect of gate bias depletes only the region at the oxide interface (≈1 μm in depth; details are provided in the Supporting Information) and noticeable dark leakage current can be observed.[47]

Figure 4b illustrates the tuning of the operation mode under various illumination wavelengths. For illumination with a short wavelength, a large amount of optically excited carriers generated due to the high absorption coefficient. The phototransistor easily operates in the on-state mode. The negative V_{GS} shows negligible influence on the photocurrent while exhibits a significant restraint to the dark current. For illumination with a longer wavelength, decreased absorption coefficient in Si-NM leads to an insufficient accumulation of photon-generated carriers in the channel, causing smaller photocurrent. The evolution of responsivity under different wavelengths agrees well with the fluctuations in the responsivity spectrum (Figure 3a). Output curves in Figure 4c,d display the I_{DS}–V_{DS} characteristics of the device at V_{GS} = 0 and −3 V, respectively. When the gate voltage is zero or positive (>V_T), both photocurrent and dark current are in the same order of magnitude. The phototransistor shows high responsibility, but a limited photo-to-dark current ratio. When the gate voltage is −3 V (<V_T), the phototransistor becomes quite sensitive even under longer wavelength illumination. The tuning of gate bias enables expediently switching of the operation mode according to requirements.

2.4. Bendability

Apart from the excellent optoelectronic properties described above, the ultrathin thickness of Si-NM significantly reduces

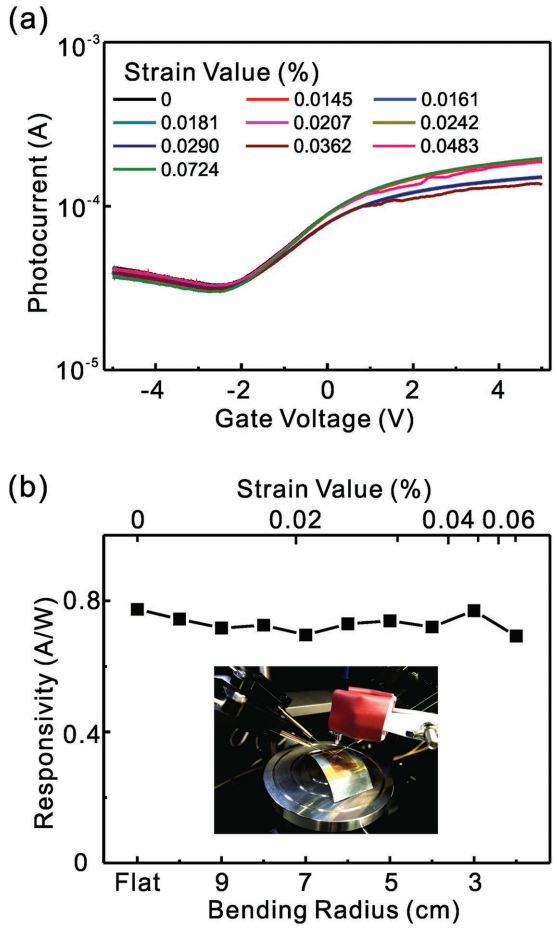

Figure 5. Evolution of optoelectronic characterization under bending condition. a) Photocurrent of the device as a function of gate voltage under different bending strain values. V_{DS} is kept constant at 0.1 V. The wavelength and intensity of the illumination are 405 nm and 5.5 mW mm^{-2}, respectively. b) The responsivity of the device under different bending conditions (V_{GS} = −3 V and V_{DS} = 0.1 V). The inset is the experimental configuration used to characterize a bent device.

the strain applied to the device in the bent state.[7] This mechanical property enables silicon-based electronics to have the comparable flexibility to organic semiconductors. With the accompanying of the flexible transient layer (PAMS) and polymer substrate (Kapton film), our Si-NM phototransistor thus can work in bending conditions. **Figure 5**a displays the gate bias modulated photocurrent of the phototransistor under different bending conditions. The electronic performance of the device in dark is presented in the Supporting Information (Figure S5, Supporting Information). In this backward bending characterization, the Si-NM functional layer on top surface suffers from tensile strain. The strain values can be estimated from the following equation[50]

$$strain = \frac{1}{\frac{2R}{\Delta R} + 1} \tag{3}$$

where R is the bending radius and ΔR is the total thickness of the flexible device (≈29 μm).The small fluctuation in the photocurrent verifies the good stability of the flexible phototransistor. Figure 5b shows the influence of the bending condition on the responsivity of the device under high photo-to-dark current ratio mode (V_{GS} = −3 V, V_{DS} = 0.1 V). The responsivity maintains at a high level at various bending state, which proves that the device has potential in flexible electronics.

2.5. Thermally Triggered Transient Process

The thermally degradable functionality of Si-NM phototransistor depends on the pyrolysis character of PAMS interlayer below. When heated to a temperature above a critical value, PAMS degrades into volatile products with a rapid "unzipping" decomposition process (Figure S6a, Supporting Information).[51] This decomposition kinetic depends largely on the molecular weight and molecular distribution of PAMS.[52] Figure S6b (Supporting Information) illustrates the thermal decomposition property of PAMS employed in this work. The thermal gravimetric analysis carried out at an increasing rate of 10 °C min^{-1} shows that the decomposition begins at ≈250 °C and completes at ≈315 °C with nearly 100% degradation rate (Figure S6b, Supporting Information). The maximum slope reveals the peak degradation rate exists at ≈285 °C. Such thermal analysis indicates the PAMS interlayer can be used in phototransistor device for the purpose of producing transient component that works properly at relatively high temperature.

Figure 6a reveals the ability of gate modulation to the phototransistor at elevated temperatures. The Si-NM phototransistor exhibits effective gate controllability from room temperature (RT) to 150 °C, and noticeable gate controllability still exists at 250 °C. One can see that when the temperature is below PAMS degradation temperature, the gate modulated off-state current raises with the temperature while the on-state current exhibits an inverse behavior. In the off-state, the leakage current mainly comes from the reverse current of the p–n junction in the phototransistor, which is mainly decided by the intrinsic carrier concentration.[53] Thus the significant increase of intrinsic carrier density at high temperature dramatically increases the dark current of the phototransistor. In the on-state, the inversion of channel leads to a lateral n^+–n–n^+ conducting structure. The reduced on-state current at high temperature is mainly due to the decrease of carrier mobility with temperature.[54] Fortunately, this temperature induced functional degradation in Si-NM devices is much smaller than bulk ones because of the elimination of vertical p–n junction in source/drain regions to the substrate.[55] Therefore, the Si-NM is more compatible to high-temperature applications. Moreover, the gate modulation characterized at room temperature after 250 °C baking (gray dash line) indicates that this degradation is reversible. Figure 6b further illustrates such temperature-dependent degradation behavior of the phototransistor. The dark current rises with the increase of temperature because of the degradation of gate modulation. While the photocurrent drops at a higher temperature because of the reduction of carrier mobility. This degradation of detecting performance is reversible if the baking temperature is below the critical degradation temperature of PAMS (see the gray dashed line in Figure 6b). At temperature over the critical point (e.g., 300 °C),

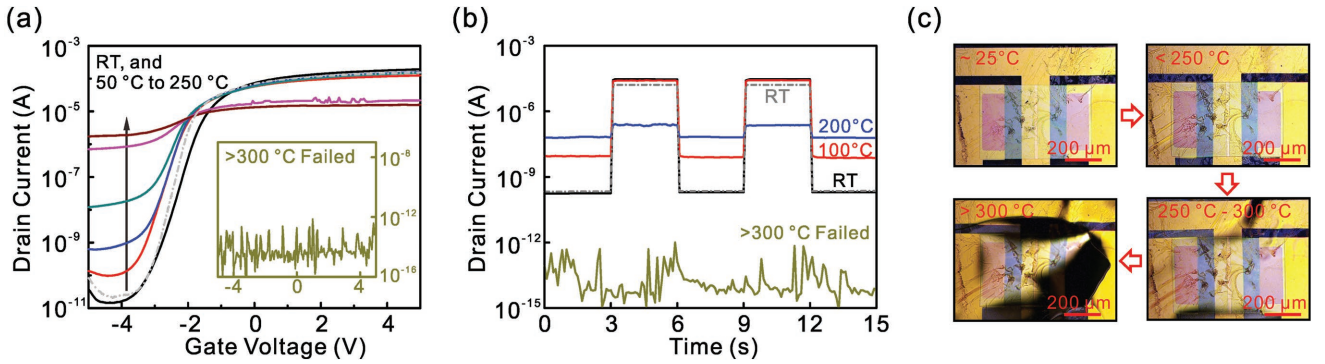

Figure 6. Temperature-dependent characterization of the transient Si-NM device. a) Real-time characterization of the gate modulation curves at room temperature (RT) and elevated temperatures from 50 to 250 °C with a step of 50 °C. The gray dashed line was collected at room temperature after the device was heated at 250 °C for 3 min. The inset shows the electric character of the device after being heated at a temperature over 300 °C for 3 min. b) Real-time characterization of the on–off optoelectronic response of the device at different temperatures. The gray dashed line was collected at room temperature after the device was heated at 250 °C for 3 min. The wavelength and intensity of the illumination are 405 nm and 5.5 mW mm^{-2}, respectively. c) Destruction of the device with the increasing temperature.

the device exhibits the electrical character of a broken circuit (inset in Figure 6a and the bottom curve in Figure 6b).

The above-mentioned irreversible electronic failure is based on the physical destruction of the device structure. Figure 6c illustrates the morphology change of the device with the increasing temperature. For temperature below 250 °C, the device shows flat surface morphology. In the temperature range of ≈250 to ≈300 °C, PAMS starts to release volatile degradation products (Figure S6, Supporting Information). The gas products concentrate below Si-NM and result in the distortion of the functional layer. For even higher temperature (>300 °C), the accumulation of volatile products yields local high pressure. As a result, the functional layer broke into separate parts (the fourth in Figure 6c), leading to irreversible functional failure of the device. Such a process usually happens within a minute at degradation temperature. The degradation process of the device over time can be found in the Supporting Information (Figure S7 and Video S1, Supporting Information). The formation of the device at high temperature also induced the destruction of SiO_2 encapsulation layer. This fragmentation process typically takes place in thin film to release deformation energy.[56,57] The fragment morphology on the device surface (Figure S8, Supporting Information) further confirms the irreversible destruction of the phototransistor.

3. Conclusion

In conclusion, we demonstrate flexible transient phototransistors by use of wafer-compatible Si-NMs and thermally degradable PAMS, which are consistent with the device-first bottom-up strategy and exhibit excellent optoelectronic characters. The effective gate modulation and full exposure of the light-sensitive channel play dominant roles in the realization of the ultrahigh photo-to-dark current ratio in the device (10^7). The degradation products of PAMS lead to a local high pressure below Si-NM, resulting in an irreversible physical destruction of the device when it is heated up to 300 °C or above. Such device design based on Si-NM and PAMS exhibits a great potential for flexible transient electronics and optoelectronics working at adopted temperature. We expected that this wafer-compatible strategy could be applicable for future advanced transient electronics, including signal processing, logic analysis, data storage, and their integration.

4. Experimental Section

Fabrication of the Phototransistor on SOI Wafer: The fabrication started with a mechanically grinding process to reduce the substrate thickness of an SOI wafer (≈700 μm thick with 340 nm thick device silicon and 2 μm thick buried oxide, weakly p-doped) to ≈200 μm. 1000 °C liquid source doping with phosphorus oxychloride and isolation with reactive ion etching (RIE) formed the source and drain regions with concentrations of ≈10^{19} cm^{-3} (Figure 1a, label I). A series of standard photolithography, isolation, dielectric oxide stack growth, etching, metallization, and annealing process completed the phototransistor array on SOI wafer (Figure 1a, label II).

Wafer-Compatible Transfer of Flexible Device: Spin-coating and curing technique formed the PAMS transient function interlayer and polyimide (PI 2000) stress buffer layer on top surface of SOI wafer (Figure 1a, label III) in turn. A 12.5 μm thick Kapton film coated with 20 nm SiO_2 and 5 μm adhesive layer served as the final flexible substrate. Pressure-assisted bonding process stuck the front side of SOI on the flexible substrate and laminated the whole structure on a temporary glass support (coated with 10 μm polydimethylsiloxane). After bonding, inductively coupled plasma reactive ion etching (ICP-RIE, Oxford, Plasma Lab ICP 180) process with SF_6/O_2 removed the silicon substrate of SOI wafer. At last, CF_4/O_2 RIE dry etching followed by buffered oxide wet etching achieved contact lead for metal electrodes through the buried oxide layer. Peeling the device from the temporary substrate yielded the final flexible Si-NM phototransistor (Figure 1a, label IV). This back side etching process could cause a rough surface to the SiO_2 encapsulation layer on device surface with a root-mean-square roughness of ≈5.85 nm (see also Figure S1 of the Supporting Information). Since the SiO_2 encapsulation layer and polymer substrate prevented Si-NM from interaction with etching gas, the back side etching process had negligible influence on the performance of the device (see also Figure S2 of the Supporting Information).

Characterization: The electronic properties were characterized by a semiconductor analyzer (Keithley 4200A). The single wavelength illumination was provided with a semiconductor laser (Xi'an Lei Ze Electronic Technology Co., Ltd, 405 nm). The irradiation power was calibrated with an optical power meter. The photocurrent on–off speed was characterized by a digital oscilloscope (Tektronix MSO54). The

405 nm semiconductor laser equipped with an optical chopper (SR 540) provided purse irradiation. In the spectrum response characterization, the light source was provided by a supercontinuum source (SC-PRO, YSL Photonics Inc.) equipped with a filter system (AOTF-Pro, YSL Photonics Inc.). The photocurrent was recorded by the semiconductor analyzer. In the optoelectronic performance under bending state, the phototransistor was stuck on a curved iron sheet with a certain diameter on the probe station. In the temperature-dependent electronic and optoelectronic characterization, a hot plate was used to heat the device.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the Natural Science Foundation of China (Grant Nos. U1632115 and 51602056), the Science and Technology Commission of Shanghai Municipality (Grant Nos. 17JC1401700 and 18ZR1405100), the National Key Technologies R&D Program of China (Grant No. 2015ZX02102-003), and the Changjiang Young Scholars Program of China. Part of the experimental work was carried out in Fudan Nanofabrication Laboratory.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

flexible phototransistors, high temperature, poly-α-methylstyrene, silicon nanomembranes, transient electronics

Received: July 28, 2018
Revised: September 11, 2018
Published online: October 10, 2018

[1] H. Fang, K. J. Yu, C. Gloschat, Z. Yang, C. H. Chiang, J. Zhao, S. M. Won, S. Xu, M. M. Trumpis, Y. Zhong, E. Song, S. W. Han, Y. Xue, D. Xu, G. Cauwenberghs, M. Kay, Y. Huang, J. Viventi, I. R. Efimov, J. A. Rogers, *Nat. Biomed. Eng.* **2017**, *1*, 0038.
[2] Y. K. Lee, K. J. Yu, E. M. Song, A. B. Farimani, F. Vitale, Z. Xie, Y. Yong, Y. Kim, A. Richardson, H. Luan, Y. Wu, X. Xie, T. H. Lucas, K. Crawford, Y. F. Mei, X. Feng, Y. Huang, B. Litt, N. R. Aluru, L. Yin, J. A. Rogers, *ACS Nano* **2017**, *11*, 12562.
[3] M. Kim, J. H. Seo, Zhao, D. S. C. Liu, K. Kim, K. Lim, W. Zhou, E. Waks, Z. Q. Ma, *J. Mater. Chem. C* **2017**, *5*, 264.
[4] G.-T. Hwang, D. Im, S. E. Lee, J. Lee, M. Koo, S. Y. Park, S. Kim, K. Yang, S. J. Kim, K. Lee, K. J. Lee, *ACS Nano* **2013**, *7*, 4545.
[5] J. L. Hou, A. Fischer, S. C. Yang, J. Benduhn, J. Widmer, D. Kasemann, K. Vandewal, K. Leo, *Adv. Funct. Mater.* **2016**, *26*, 5741.
[6] C. H. Lin, D. S. Tsai, T. C. Wei, D. H. Lien, J. J. Ke, C.-H. Su, J.-Y. Sun, Y.-C. Liao, J. H. He, *ACS Nano* **2017**, *11*, 10230.
[7] J. A. Rogers, M. G. Lagally, R. G. Nuzzo, *Nature* **2011**, *477*, 45.
[8] Y. H. Jung, T.-H. Chang, H. L. Zhang, C. Yao, Q. Zheng, V. W. Yang, H. Mi, M. Kim, S. J. Cho, D.-W. Park, H. Jiang, J. Lee, Y. Qiu, W. Zhou, Z. Cai, S. Gong, Z. Q. Ma, *Nat. Commun.* **2015**, *6*, 7170.
[9] K. Zhang, J.-H. Seo, W. Zhou, Z. Ma, *J. Phys. D: Appl. Phys.* **2012**, *45*, 143001.
[10] P. Feng, I. Monch, G. S. Huang, S. Harazim, E. J. Smith, Y. F. Mei, O. G. Schmidt, *Adv. Mater.* **2010**, *22*, 3667.
[11] J.-H. Seo, K. Zhang, M. Kim, D. Zhao, H. Yang, W. D. Zhou, Z. Q. Ma, *Adv. Opt. Mater.* **2016**, *4*, 120.
[12] M. M. Roberts, L. J. Klein, D. E. Savage, K. A. Slinker, M. Friesen, G. Celler, M. A. Eriksson, M. G. Lagally, *Nat. Mater.* **2006**, *5*, 388.
[13] E. Menard, K. J. Lee, D. Y. Khang, R. G. Nuzzo, J. A. Rogers, *Appl. Phys. Lett.* **2004**, *84*, 5398.
[14] E. M. Song, Q. L. Guo, G. S. Huang, B. Jia, Y. F. Mei, *ACS Appl. Mater. Interfaces* **2017**, *9*, 12171.
[15] A. M. Hussain, M. M. Hussain, *Adv. Mater.* **2016**, *28*, 4219.
[16] A. Gumus, A. Alam, A. M. Hussain, K. Mishra, I. Wicaksono, G. A. T. Sevilla, S. F. Shaikh, M. Diaz, S. Velling, M. T. Ghoneim, S. M. Ahmed, M. M. Hussain, *Adv. Mater. Technol.* **2017**, *2*, 1600264.
[17] Y. Gao, K. Sim, X. Yan, J. Jiang, J. Xie, C. Yu, *Sci. Rep.* **2017**, *7*, 947.
[18] K. K. Fu, Z. Wang, J. Dai, M. Carter, L. Hu, *Chem. Mater.* **2016**, *28*, 3527.
[19] S. W. Hwang, H. Tao, D. H. Kim, H. Y. Cheng, J. K. Song, E. Rill, M. A. Brenckle, B. Panilaitis, S. M. Won, Y. S. Kim, Y. M. Song, K. J. Yu, A. Ameen, R. Li, Y. W. Su, M. M. Yang, D. L. Kaplan, M. R. Zakin, M. J. Slepian, Y. G. Huang, F. G. Omenetto, J. A. Rogers, *Science* **2012**, *337*, 1640.
[20] R. K. Pal, S. C. Kundu, V. K. Yadavalli, *ACS Appl. Mater. Interfaces* **2018**, *10*, 9620.
[21] S. K. Kang, R. K. J. Murphy, S. W. Hwang, S. M. Lee, D. V. Harburg, N. A. Krueger, J. H. Shin, P. Gamble, H. Y. Cheng, S. Yu, Z. J. Liu, J. G. McCall, M. Stephen, H. Z. Ying, J. Kim, G. Park, R. C. Webb, C. H. Lee, S. J. Chung, D. S. Wie, A. D. Gujar, B. Vemulapalli, A. H. Kim, K. M. Lee, J. J. Cheng, Y. G. Huang, S. H. Lee, P. V. Braun, W. Z. Ray, J. A. Rogers, *Nature* **2016**, *530*, 71.
[22] B. H. Kim, J.-H. Kim, L. Persano, S.-W. Hwang, S. Lee, J. Lee, Y. Yu, Y. Kang, S. M. Won, J. Koo, Y. K. Cho, G. Hur, A. Banks, J.-K. Song, P. Won, Y. M. Song, K.-I. Jang, D. Kang, C. H. Lee, D. Pisignano, J. A. Rogers, *Adv. Funct. Mater.* **2017**, *27*, 1606008.
[23] C. W. Park, S. K. Kang, H. L. Hernandez, J. A. Kaitz, D. S. Wie, J. Shin, O. P. Lee, N. R. Sottos, J. S. Moore, J. A. Rogers, S. R. White, *Adv. Mater.* **2015**, *27*, 3783.
[24] H. L. Hernandez, S. K. Kang, O. P. Lee, S. W. Hwang, J. A. Kaitz, B. Inci, C. W. Park, S. J. Chung, N. R. Sottos, J. S. Moore, *Adv. Mater.* **2014**, *26*, 7637.
[25] W. Zhang, M. Chan, S. K. H. Fung, P. K. Ko, *IEEE Electron Device Lett.* **1998**, *19*, 435.
[26] B. R. Huang, D. K. Reinhard, *Appl. Phys. Lett.* **1991**, *59*, 1494.
[27] T. Ono, N. Itabashi, I. Ochiai, S. Yamamoto, K. Mochiji, *Jpn. J. Appl. Phys.* **1997**, *36*, 6718.
[28] R. Fuller, H. Evans, W. H. Speece, D. DeCrosta, R. Lowry, *IEEE Trans. Nucl. Sci.* **1997**, *44*, 1834.
[29] B. K. Ip, K. C. Kao, D. J. Thomson, *Solid-State Electron.* **1991**, *34*, 123.
[30] D. K. Schroder, *Semiconductor Material and Device Characterization*, John Wiley & Sons, Hoboken, NJ, USA **2006**, Ch. 8.
[31] D. Hoyniak, E. Nowak, R. L. Anderson, *J. Appl. Phys.* **2000**, *87*, 876.
[32] D. Liu, W. D. Zhou, Z. Q. Ma, *Photonics* **2016**, *3*, 40.
[33] D. M. Pai, *J. Appl. Phys.* **1975**, *46*, 5122.
[34] H. S. Kang, C. S. Choi, W. Y. Choi, D. H. Kim, K. S. Seo, *Appl. Phys. Lett.* **2004**, *84*, 3780.
[35] V. N. Tran, R. Stuart, H. Bhavsar, *Phototransistor Switching Time Analysis, AN3009*, California Eastern Laboratories, CA, USA **2009**, p. 1.
[36] L. Huang, W. C. Tan, L. Wang, B. Dong, C. Lee, K.-W. Ang, *ACS Appl. Mater. Interfaces* **2017**, *9*, 36130.
[37] R. K. Chowdhury, R. Maiti, A. Ghorai, A. Midya, S. K. Ray, *Nanoscale* **2016**, *8*, 13429.

[38] F. Schuster, D. Coquillat, H. Videlier, M. Sakowicz, F. Teppe, L. Dussopt, B. Giffard, T. Skotnicki, W. Knap, *Opt. Express* **2011**, *19*, 7827.
[39] J. P. Zheng, K. L. Jiao, W. P. Shen, W. A. Anderson, H. S. Kwok, *Appl. Phys. Lett.* **1992**, *61*, 459.
[40] Si photodiodes, https://www.hamamatsu.com/resources/pdf/ssd/e02_handbook_si_photodiode.pdf, (accessed: September 2018).
[41] M. Dang, H.-C. Yuan, Z. Ma, J. Ma, G. Qin, *Appl. Phys. Lett.* **2017**, *110*, 253104.
[42] S. A. Scott, W. Peng, A. M. Kiefer, H. Jiang, I. Knezevic, D. E. Savage, M. A. Eriksson, M. G. Lagally, *ACS Nano* **2009**, *3*, 1683.
[43] W. C. Dash, R. Newman, *Phys. Rev.* **1955**, *99*, 1151.
[44] G. J. Li, Q. L. Guo, Y. F. Fang, S. W. Tang, M. J. Liu, G. S. Huang, Y. F. Mei, *Phys. Status Solidi A* **2017**, *214*, 1700295.
[45] M.-Y. Hwang, H. Kim, E.-S. Kim, J. Lee, S.-M. Koo, *Nanoscale Res. Lett.* **2011**, *6*, 573.
[46] E. M. Song, W. P. Si, R. G. Cao, P. Feng, I. Monch, G. S. Huang, Z. F. Di, O. G. Schmidt, Y. F. Mei, *Nanotechnology* **2014**, *25*, 485201.
[47] D. Kufer, G. Konstantatos, *ACS Photonics* **2016**, *3*, 2197.
[48] B. Dalla, G. U. Pignatel, G. Verzellesi, P. Bellutti, M. Boscardin, L. Ferrario, N. Zorzi, A. Maglione, *Microelectron. J.* **1998**, *29*, 49.
[49] H. Yamamoto, K. Taniguchi, C. Hamaguchi, *Jpn. J. Appl. Phys.* **1996**, *35*, 1382.
[50] F. Balestra, *Solid-State Electron.* **1992**, *35*, 1783.
[51] S. L. Malhotra, C. Baillet, L. Minh, L. P. Blanchard, *J. Macromol. Sci., Part A: Chem.* **1978**, *12*, 129.
[52] J. M. G. Cowie, S. Bywater, *J. Polym. Sci., Part A: Polym. Chem.* **1961**, *54*, 221.
[53] Y. Murakami, T. Shingyouji, *J. Appl. Phys.* **1994**, *75*, 3548.
[54] P. G. Neudeck, R. S. Okojie, L. Y. Chen, *Proc. IEEE* **2002**, *90*, 1065.
[55] M. A. Huque, S. K. Islam, L. M. Tolbert, B. J. Blalock, *IEEE Trans. Power Electron.* **2012**, *27*, 4153.
[56] G. J. Li, E. M. Song, G. S. Huang, Q. L. Guo, F. Ma, B. Zhou, Y. F. Mei, *Adv. Funct. Mater.*, https://doi.org/10.1002/adfm.201801448.
[57] Z. Qin, N. M. Pugno, M. J. Buehler, *Sci. Rep.* **2015**, *4*, 4966.

