

Artificial neuron synapse transistor based on silicon nanomembrane on plastic substrate*

Minjie Liu¹, Gaoshan Huang^{1,†}, Ping Feng^{2,†}, Qinglei Guo¹, Feng Shao², Ziao Tian¹, Gongjin Li¹, Qing Wan², and Yongfeng Mei¹

¹Department of Materials Science, Fudan University, Shanghai 200433, China

²School of Electronic Science and Engineering and Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing 210093, China

Abstract: Silicon nanomembrane (SiNM) transistors gated by chitosan membrane were fabricated on plastic substrate to mimic synapse behaviors. The device has both a bottom proton gate (BG) and multiple side gates (SG). Electrical transfer properties of BG show hysteresis curves different from those of typical SiO₂ gate dielectric. Synaptic behaviors and functions by linear accumulation and release of protons have been mimicked on this device: excitatory post-synaptic current (EPSC) and paired pulse facilitation behavior of biological synapses were mimicked and the paired-pulse facilitation index could be effectively tuned by the spike interval applied on the BG. Synaptic behaviors and functions, including short-term memory and long-term memory, were also experimentally demonstrated in BG mode. Meanwhile, spiking logic operation and logic modulation were realized in SG mode.

Key words: silicon nanomembrane; chitosan membrane; excitatory post-synaptic current

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1. Introduction

Over 10^{11} neurons are highly interconnected by about 10^{15} synapses in neural networks of the human brain. Neuron synaptic transmission has been recognized early as a key property of brain function likely to underlie learning, memory and reaction to our environment^[1,2]. Synaptic intensity can be precisely adjusted by the concentrations of ionic species which plays as the connection between presynaptic and postsynaptic neurons^[3].

Through a single synapse, a potential spike signal from a presynaptic neuron can trigger an ionic excitatory postsynaptic current (EPSC) that lasts for 1– 10^4 ms in a postsynaptic neuron^[4]. Processing and integration of neuron network inputs often result in short-term memory (STM) and long-term memory (LTM) behavior alterations as a result of past experiences^[5,6]. Among various implementation technologies, synaptic electronics is an emerging technology aimed at facilitating neuromorphic computing through the use of bio-inspired hardware systems^[7]. A proper device to mimic the neuron network and synapse process has become the key to neural engineering. These devices should have high sensitivity and low energy assumption. More importantly, the EPSC behavior should be close to the real neuron synapse behavior biologically. In this sense, conventional CMOS synaptic devices, such as SRAM, SDRAM and analog floating-gate transistor^[8–10], occupy large size or consume high energy, as well as lack the plastic property. By using lowpower very large scale integration (VLSI) array to mimic neurons of spike-timing dependent plasticity is a useful way of mimicking neuron synapse, but the

method still faces the problem of connecting too many wires and layouts and the devices are not flexible^[11].

Transistors gated by proton gates play an important role in artificial synapse networks. Researches show that strong lateral modulation is observed due to the proton-related electrical double-layer (EDL) effect in in-plane lateral-coupled oxide-based artificial synapse network coupled by proton neurotransmitters^[12]. In electrolyte-gated field effect transistors (FETs), ions would migrate to the channel/electrolyte interface when an appropriate voltage is applied on the gate electrode^[13]. Recently, researchers have tried indium-zinc-oxide as the channel material coupling EDL with proton gates for the emulation of artificial neuron systems^[14,17]. On the other hand, chitosan has wide applications in biosensors, proton exchange films, and artificial skin. It has good performance with high proton conductivity and large specific capacitance prepared by a simple coating-peeling process^[18–20]. For the integrated circuit industry, silicon remains the most commonly used material. Combining silicon into synaptic electronics will make the artificial synapse network more compatible to neuromorphic computing. Especially, silicon nanomembranes (SiNMs) are very thin, large, free-standing or free-floating two-dimensional (2D) structures that can variously be flat, rolled into tubes, made into any number of odd shapes, cut into millions of identical wires, used as conformal sheets, or chopped into tiny pieces^[21]. Realized by silicon-on-insulator (SOI) technology, SiNMs have shown great promise in a variety of applications such as flexible and stretchable electronics and optoelectronics, and as the base to create identical Si

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† Corresponding author. Email: gshuang@fudan.edu.cn, pfeng@nju.edu.cn

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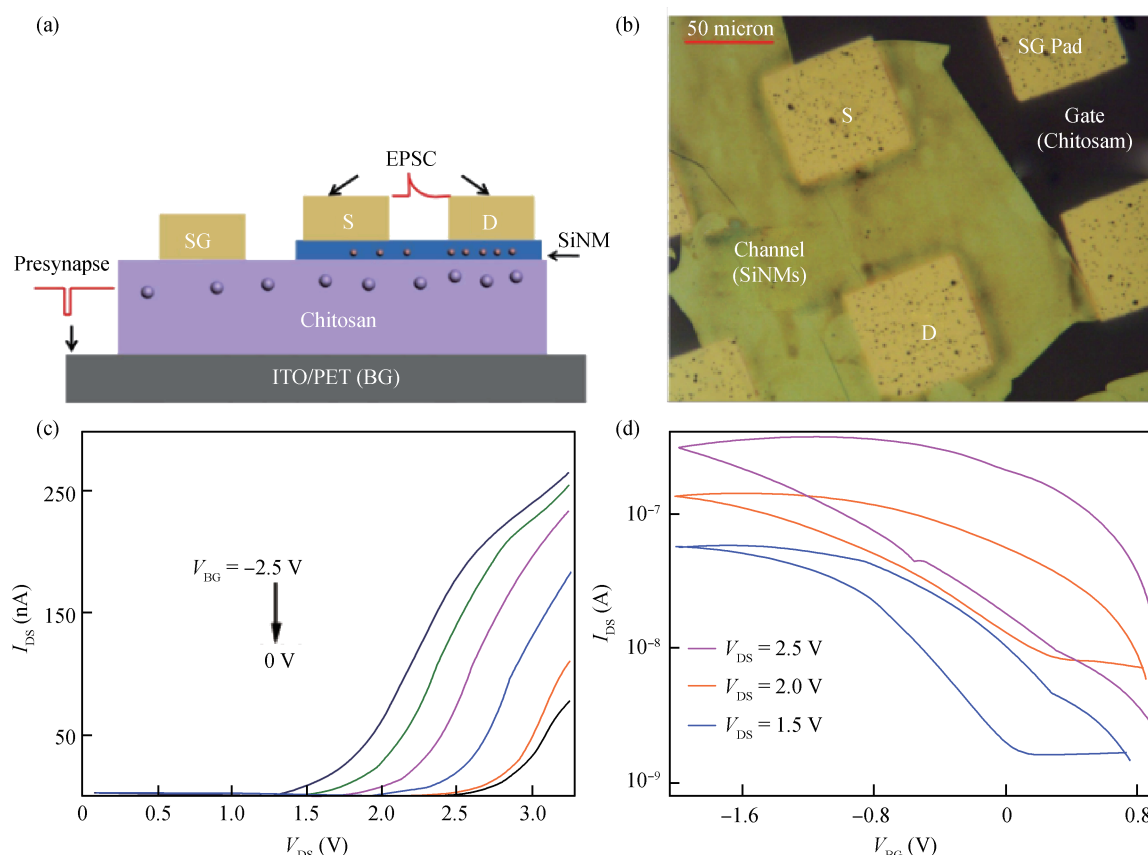


Fig. 1. (Color online) (a) Schematic diagram of SiNM transistors gated by chitosan membrane at BG test mode. The balls represent holes in SiNM. (b) Optical microscope image of the devices. (c) Output curves with different BG voltages (V_{BG} , step: 1 V). (d) Transfer curves I_{DS} – V_{BG} with different V_{DS} .

nanowires for chemical and bio-sensor^[22,23]. HF etching on SOI has been proven to be a proper way to transfer SiNMs on flexible substrates for flexible and wearable electronic devices^[24].

Here, we combined SiNMs with chitosan proton gate on the ITO/PET substrate. This device offers multiple gates for the SiNM channel. Our device can mimic the EPSC properly at back gate (BG) mode. Synaptic behaviors and functions, such as paired-pulse facilitation (PPF), STM, and STM turning to LTM are experimentally demonstrated. The multiple-gates SiNM synaptic transistors may find potential applications in biochemical sensors for dendritic integration and neuromorphic systems with an easy and large area fabrication process. The plastic substrate used in this work may also pave the way for realization of flexible and wearable devices.

2. Experiment and results

2.1. Fabrication and electric curve

Figs. 1(a) and 1(b) are the schematic diagram and microscope image of SiNMs transistors gated by chitosan proton on the PET/ITO substrate.

SiNM-based synaptic transistors on chitosan membrane were fabricated at room temperature. Chitosan solution (2 wt% in acetic acid) was dropped onto the ITO/PET flexible substrate. The obtained chitosan solution was dried at room tem-

perature for 24 h to form a homogeneous solid chitosan membrane. Such a membrane on flexible substrate could act as mechanical support and as gate dielectrics for SiNM synaptic transistors. Meanwhile, we etched the SiO_2 layer in SOI to get free standing SiNM, which were then transferred onto chitosan membrane by a thermal-tape-release approach to get the SiNM channel on the chitosan gate^[25]. Finally, Cr/Au (10 nm/100 nm) patterns were deposited on the SiNM by electron beam with a shadow mask. It could be seen from Fig. 1(b) that Cr/Au pads are grown right above the SiNM, which can be used as sources and drains of our device. While the Cr/Au pads located right on chitosan beside SiNMs can be regarded as SGs. Given that the ITO/PET substrate is highly electric conductive, it can be regarded as gate electrode of BG. In this way, there are two kinds of gates in our transistor: BG (i.e., ITO/PET for each single SiNM device) and SG (i.e., Cr/Au multiple gates on side of SiNM). Fig. 1(c) illustrates the output curve when the voltage is applied on the BG. The I_{DS} – V_{DS} curves are typical for FET. If we turn the BG voltage to negative, the holes in our near-intrinsic p-type SiNM channel accumulate at the SiNM/chitosan interface gradually. The increase of negative voltage causes an accumulation of holes at the bottom of SiNM (Fig. 1(a)), which results in a decrease of the threshold voltage. From Fig. 1(c), one can see that the threshold voltage of our transistor decreases about 1.5 V when the BG voltage changes from 0 to –2.5 V. Fig. 1(d) shows the transfer curve at different gate voltages (V_{BG}) under three dif-

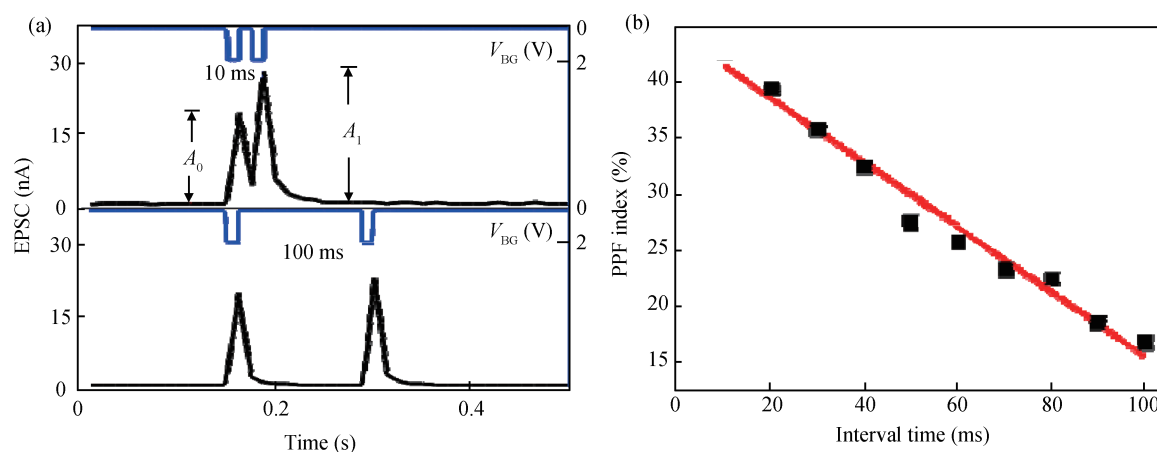


Fig. 2. (a) EPSCs triggered by two successive presynaptic spikes when successive pulses of different interval times (10 and 100 ms) were applied on the BG with $V_{DS} = 2$ V. Here we define the PPF index as $(A_1 - A_0)/A_0$. (b) PPF index measured at different interval times. The red line is the linear fitting result.

ferent V_{DS} . Due to the distributions of protons in the chitosan electrolyte layer, an electrical hysteresis curve can be seen in Fig. 1(d). With decreasing (i.e., from positive to negative) V_{BG} in the loop direction, negative charges are trapped inside of the chitosan gate and protons are moving away from the interface of chitosan/SiNM, negative charges will induce holes in the P-type SiNM surface (Fig. 1(a)), resulting in an increase in I_{DS} with electron conduction. With increasing V_{BG} (i.e., from negative to positive), the protons are not accumulated to the interface at once, still inducing the certain amount of holes at the SiNM surface for a certain time, which explains the hysteresis phenomenon. The area of the loop increases when the V_{DS} gets larger, indicating that there is a surface planar electric field when the drain voltage is applied. The V_{DS} applied causes not only the current in the SiNM but also a surface planar electric field at the SiNM/chitosan interface because the SiNM is very thin (50 nm). When V_{DS} is positive, there will be more protons near the source in the proton gate at the SiNM/chitosan interface, causing there to be more time to accumulate holes. The higher the drain voltage is, the more time it takes to accumulate the protons, which cause the large area of the loop.

2.2. EPSC mimicking at BG mode

When a presynaptic spike is applied on the BG, protons will migrate to the chitosan/SiNM interface and trigger a post synapse current between source and drain, which can be regarded as an EPSC signal.

Fig. 2(a) shows typical EPSCs triggered by two successive presynaptic spikes with an inter-spike interval of 10 and 100 ms respectively. The PPF on the chitosan-gated device in BG mode can be observed. Postsynaptic current is measured from the SiNMs channel layer at a constant $V_{DS} = 2.5$ V (the black line) when two pulses (the blue line) are applied on the BG electrode. Here, we define the amplitude of EPSC triggered by the second presynaptic spike as the PPF index, which can be calculated as $(A_1 - A_0)/A_0$, where A_0 is the first EPSC intensity and A_1 is the second EPSC intensity. To investigate the influence of the second presynapse applied on the BG to PPF

of the synaptic transistor, a series of successive pulses of different interval times (10–100 ms, 10 ms step) were applied on the gate. Fig. 2(b) shows the change of PPF index at different presynapse interval times. We know that chitosan is a linear bio-polysaccharide composed of randomly distributed b-(1-4) linked D glucosamine (deacetylated unit) and N-acetyl-D-glucosamine (acetylated unit)^[26] and therefore the PPF index decreases with the increase of spike width linearly in the chitosan-gated device^[20]. The PPF index reaches a maximum value of ~42% when the interval time is 10 ms and it decreases to near 17% when the pulse interval is long enough (e.g., 100 ms). This behavior is similar to the real EPSC behavior^[27]. In the present case, the migration of protons in the chitosan membrane plays an important role for EPSC triggering, and the increase of channel current is due to the proton migration and interfacial EDL electrostatic modulation^[28]. When the interval time is short, the protons triggered by the first spike still partially accumulate at the interface of the chitosan/SiNMs channel when the second spike comes. The total amount of the accumulated protons will get larger due to the integrated effect. While for a long interval time, the protons triggered by the first spike will diffuse back to the equilibrium position, causing the summation effect to disappear and the PPF index to decrease^[12].

Learning process is one of the key properties for biological synapse behavior. For memory behavior, the intensity of the last EPSC signal is influenced by the previous signal. To further study the memory behavior in our device, we put 12 gate spikes (−2.0 V, 10 ms) on the back gate and found a linear increased PPF signal, as shown in Fig. 3(a).

The time-dependent channel EPSC behaviors can be regarded as a memory behavior. PPF is thus a form of short-term synaptic plasticity associated with short-term adaptations to sensory inputs, and short-lasting forms of memory^[3]. Synaptic memory behaviors like the EPSC signals increase by presynaptic spike width from 10 to 80 ms is shown in Fig. 3(b) at the BG mode. When the stimulation pulse width is increased, an obvious enhancement in I_{DS} is observed. At a larger spike width, the process of increasing relaxation time can be regarded as a proper way of turning STM to LTM^[29].

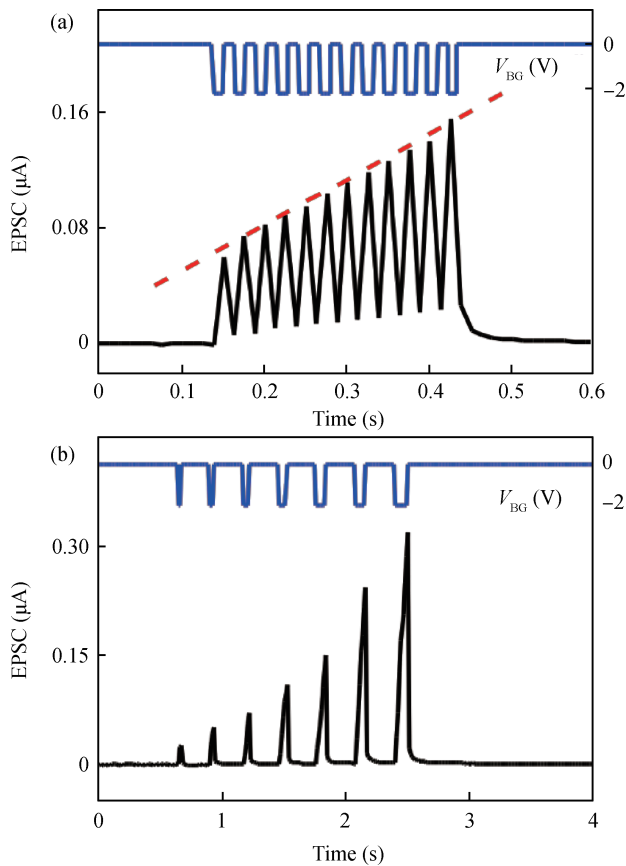


Fig. 3. (a) EPSC responses of device to the stimulus train with a 12 gate spikes (-2.0 V, 10 ms). The V_{DS} is fixed at 2.5 V. (b) The width of the presynapse spike on the gate electrode was changed from 10 to 80 ms.

2.3. EPSC integration at SG mode

To further investigate the synaptic integration in neuron network, we applied presynaptic spikes on multiple SGs.

The test mode is shown in Fig. 4(a). In Fig. 4(b), we found that EPSC signal changes linearly not only by presynapse time change at the BG mode (time domain in Fig. 3), but also increases linearly by gates spikes input at the SG mode (space domain). When three different presynapses (-1.0 , -3.0 , and -3.0 V) are applied on the three individual SGs time by time, linear accumulation EPSCs signal can be captured with each side gate spike. Fig. 4(b) illustrates the EPSCs measured with spikes on multiple SGs. The intensity of spike 1 is -1 V, and those of spike 2 and 3 are both -3 V. Corresponding currents of spike 1, spike 2 and spike 3 were measured to be 0.51, 1.48, and 1.54 nA respectively. The arithmetic sum of spike 1 and spike 2 is 1.99 nA, and we found that the measured sum is 2.05 nA. The arithmetic sum of the amplitudes of EPSCs triggered by three spikes (spike 1, spike 2 and spike 3) is 3.53 nA and the measured amplitude is 3.59 nA, indicating the linear synaptic integration. Here, each presynaptic input can be coupled to the SiNM channel by the protons in the chitosan membranes. It is worth noting that neurons receive thousands of synaptic inputs arriving at different dendritic locations, and these synaptic inputs are integrated in the neurons and triggered local outputs^[20, 20, 31] which can be easily mimicked by SG mode in our

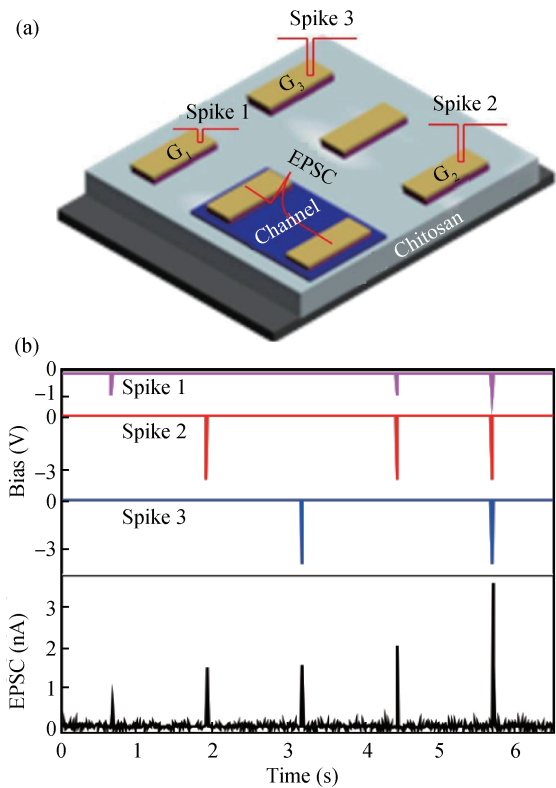


Fig. 4. (a) Schematic diagram of SiNM transistors gated by chitosan membrane at SG test mode. (b) Input-output characteristics of the OR pulse logic tuned by negative spikes applied on the controlled SGs. EPSC signal changes linearly by multiple SGs.

chitosan-gated device.

In electronic engineer aspect, the “OR” logic function can be demonstrated by our device when negative spikes are applied on the SG. When an input spike is applied on each presynaptic input terminals (spike 1, spike 2 and spike 3), a post-synaptic spike current can be measured, thus an “OR” logic function is demonstrated. There is no complex hardware connection or layout due to the strong protonic/electronic coupling effect even if we put multiple inputs on the SGs. For a single EPSC signal, the energy consumption can be roughly estimated by Joule theorem: $W = I_{\text{peak}} t V_{DS}$, where I_{peak} is the intensity of EPSC signal and t is the lasting time of the signal, respectively^[20]. For our device working at SG mode, the energy consumption of a single spike event is estimated to be as low as ~ 30 pJ when the intensity of input presynapse is -2 V. The value is much lower than the energy consumption of the conventional CMOS circuit^[11]. This result could be important for the integration of low energy cost synaptic electronics and neuromorphic systems in the future.

3. Conclusion

In this work, we have fabricated SiNM-based devices gated by the chitosan layer. Our device can be regarded as presynapse and postsynapse mimicking devices. Presynaptic spike duration time-dependent EPSCs are observed in such synaptic transistors. Proton migration triggered by the gate pulse results in the establishments of the inter-coupling between in-plane gates and the SiNM channel. STM behavior was

demonstrated by multiple pulses and PPF experiments. For the integration of neuron synapse, we found that accumulation and release of protons in the chitosan gate is a linear change over time and space. Our device can also be used as an “OR” logic function for multiple input signals. There may be a wide range of applications for our device, for example, it is possible to fabricate a sheet of SiNM-based ionic sensors to demonstrate the capability of detecting the location and pressure of touch on human skin by the SOI transfer printer technology.

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