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High-Temperature-Triggered Thermally Degradable Electronics Based on Flexible Silicon Nanomembranes

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An advanced transient approach enables the sudden degradation and subsequent disappearance of device-grade electronic systems on a temporary platform with limited remains over a desired period for long-term stable operation. To satisfy the requirements for flexible devices in transient electronics capable of working at high temperature, transient Si-nanomembrane (Si-NM) electronics integrated with high-temperature degradable poly-α-methylstyrene (PAMS) are presented. Systematic experimental studies suggest that a 4 µm thick PAMS interlayer in the Si-NM device ensures stable operation below the decomposition temperature of PAMS (≈300 °C), while the device undergoes transient process when triggered at higher temperature. Experimental characterization and theoretical modeling reveal the essential properties of the flexible device and its failure mechanism. Demonstrations of such a transient component in high-temperature electronics highlight the potential advantages in the demands for circuit safeguards, information security, and sensing/control systems.

1. Introduction

Transient electronics plays a critical role in satisfying various demands ranging from healthcare implants to environment protection and hardware security systems. Such techniques are of great interest because they allow the device physically or functionally disintegrating over a controllable time period.[1,2] The most common approach for transient technique relies on the action of wet chemistries to dissolve electronic components involving semiconductors, dielectrics, metals, and polymers.[3–5] Associated representative achievements include fully biodegradable electronic implants eliminating the need for extraction and destructible memory with microfluidic systems for information security.[6,7] Despite these successes, a daunting challenge in this field is the development of the life-cycle of the wet transient process that is usually predetermined by the dissolution rate of functional material,[8] and thus limits its potentials in nonbiological applications.

Recently, dry transient electronic systems with better on-demand controllability and feasibility to arid or weightless environment have attracted great interest.[9] In practice, mechanical destruction of handling substrate and chemical etching from solid attachments are the two main failure strategies for the dry process.[8,10] Because of the avoidance of prestored liquid chemical etchants in the device structures, such systems exhibit unique convenience in the prevention for sensitive data leakage and reduction of electronic waste to the external environment.[11–13] In fact, the technical requirements of transient systems should be changed according to specific scenarios. For example, integrated solid-state devices that operating at ambient condition higher than 150 °C exhibit promising potential in the fields of automotive, aerospace, and energy production industries.[14,15] However, combining reliable electronic performance with current transient technology at that extreme condition still remains challenging. This is mainly associated with the thermal instability of present polymer-based transient approaches.[11] To satisfy these requirements, an ideal scenario of both stimuli triggers and device structures, for these purposes, must be in consideration of restraining electrical character degradation and thermal expansion coefficient mismatch in high operating temperature.

Here, we propose novel dry transient electronics overcoming the above challenges. The integration of a sufficiently thin and high-temperature degradable poly-α-methylstyrene (PAMS) interlayer enables distinct and irreversible transient process for single crystal silicon nanomembrane (Si-NM)

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devices at its decomposition temperature (PAMS, ≈300 °C). In the flexible Si-NM based field-effect transistor (FET), reduced junction area due to ultrathin vertical dimension significantly reduces off-state leakage, which physically occurs in bulk field-effect transistors.[14] Introduction of polyimide (PI) stress buffer layer helps to weaken thermal expansion coefficient mismatch. Through these efforts, such transistor devices could meet the requirements of high-temperature electronics with stable operation below the decomposition temperature and undergo transient process when triggered at higher temperature. A combination of systematic temperature-dependent characterization, morphology analyses, and simulation reveal the theoretical failure models. This work paves the way to integrate transient technology into high-temperature flexible electronics with the potential applications of on-chip supervisory circuit safeguard, secure data storage, and sensing/control devices.

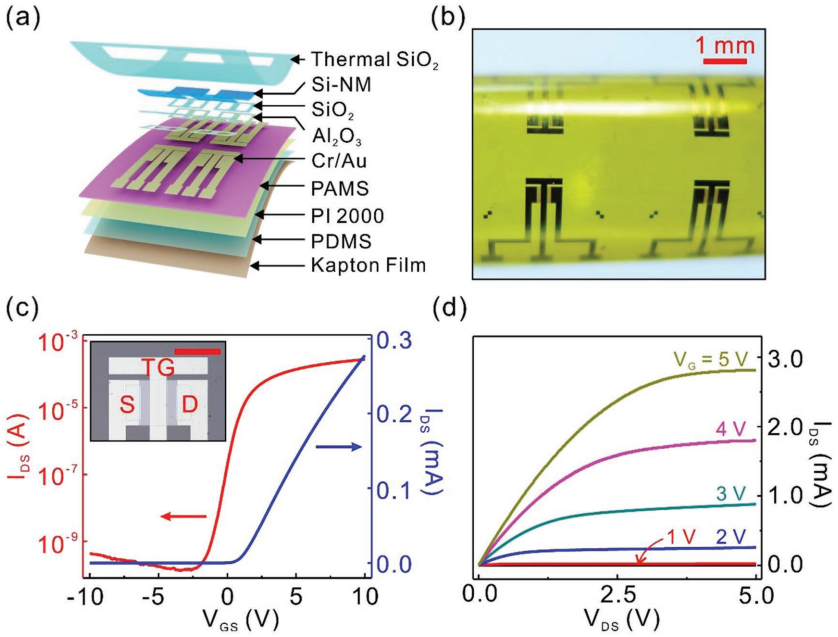

Figure 1. Structure and basic electrical properties of flexible Si-NM MOSFET. a) Schematic illustration of key functional layers of the Si-NM MOSFET in an exploded view. b) A photograph of the fabricated Si-NM MOSFET array. c) Transfer characteristics in both linear and logarithmic scales, at a supply voltage $V_{DS} = 0.1$ V. The upper inset shows an optical image of the fabricated FET. The scale bar is 400 µm. S, source; D, drain; TG, top gate. d) Output characteristics (I_{DS}–V_{DS}) of Si-NM MOSFET. From the bottom to top, V_G varies from 0 to 5 V (The curves of $V_G = 0$ V and $V_G = 1$ V are less distinct).

2. Results and Discussion

2.1. Structure and Metal Oxide Semiconductor FET (MOSFET) Characterization

Single crystal Si-NM MOSFET based on standard IC technique was fabricated and integrated into flexible device to verify the feasibility of current strategy. **Figure 1**a exhibits the multilayer configuration of Si-NM n-channel MOSFET. Thinning whole structure down to the desired thickness after the device manufacturing process is so-called device-first/bottom-up approach,[16] which is quite compatible with state-of-art IC technique. Here, the buried thermal silicon oxide layer (≈2 µm) serves as an encapsulation to the 340 nm thick Si-NM active region below. The gate dielectric stack consists of 70 nm thick SiO_2 layer and 13 nm thick Al_2O_3 layer. Photolithographically patterned Cr/Au layer (5/100 nm) defines the source, drain, and gate electrodes of the Si-NM MOSFET. PAMS (≈4 µm, Figure S1a, Supporting Information) interlayer is just below Si-NM MOSFET, and its thermally triggered decomposition behavior at particular temperature could induce mechanical destruction and thus the entire functional failure of the device-grade systems. In this multilayer structure, spin-coated and cured PI layer (≈5 µm thick) serves as the stress buffer layer. Spin-coated polydimethylsiloxane (PDMS, ≈5 µm thick) is the adhesive layer and the 12.5 µm thick Kapton film serves as a flexible substrate of the final device. Si-NM's excellent bendability, by virtue of its small thickness and polymer substrate's natural litheness, offers the whole structure with superb flexibility.[17,18] Figure 1b displays a photograph of such flexible devices with a set of Si-NM MOSFETs (curved on a plastic tube with a radius of 3 mm).

Figure 1c shows transfer characteristics of a representative Si-NM MOSFET (inset in Figure 1c, channel width $W = 400$ µm, length $L = 20$ µm. S, source; D, drain; TG, top gate) in both linear and logarithmic scale at a supply voltage $V_{DS} = 0.1$ V. Output characteristics in Figure 1d illustrates that the I_D increases with V_D in linear region and exhibits saturation behavior at high V_D (e.g., ≈4 V for $V_G = 5$ V). All these indicate the nearly-ideal MOSFET behavior under square-law theory.[19] Data from transfer characteristic and output curves direct to basic parameters of the FET (see the Supporting Information for details). The threshold voltage V_T of the FET is 0.7 V, calculating with a linear extrapolation method.[20] This transistor exhibits an on/off ratio > 10^6 with I_{on} and I_{off} of 0.27 mA and 140 pA, respectively. The peak effective carrier mobility is ≈340 cm^2 $(V\ s)^{-1}$ and the subthreshold swing is ≈300 mV. These parameters are comparable with similar transistors fabricated by conventional process.[21,22] The good performance of the current flexible device promises its important potentials in the applications of flexible high-speed logic and memory circuits.[8,23]

2.2. Integration of PAMS with Si-NM Electronics

The integration of PAMS with Si-NM electronics here (**Figure 2**a) begin with the fabrication of devices on silicon-on-insulator (SOI) wafer with standard IC process. After spin-casting and curing of PAMS and PI coating in turn on the surface of the SOI wafer, pressure bonding combines the front side with a Kapton film (≈12.5 µm thick acts as the final flexible substrate) on a temporary glass substrate. Removal of the 200 µm thick back silicon handle includes reactive ion etching (RIE, SF_6/O_2) followed by

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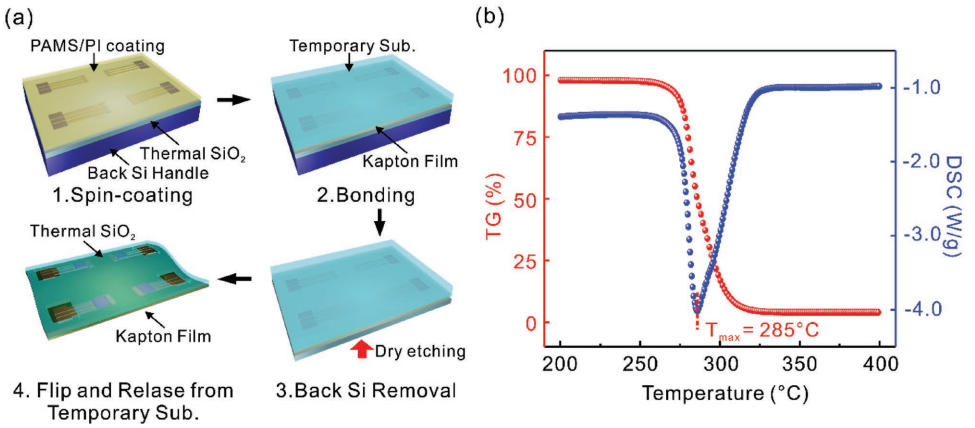

Figure 2. Materials and integration strategy for high-temperature degradable transient electronics. a) Schematic illustration of a transient Si-NM MOSFET with PAMS interlayer by the bottom-up thinning process: a-(1) Spin-casting and curing of PAMS and PI coating in turn; a-(2) Pressure bonding the top surface to a temporary glass substrate that supports a Kapton film; a-(3) Back Si handle removal by dry etching; a-(4) Release of the final flexible Si-NM MOSFET. b) TG and DSC curves of PAMS characterized in argon.

inductively coupled plasma-reactive ion etching (ICP-RIE, SF_6/O_2). The buried oxide layer (SiO_2, ≈2 µm thick) in SOI serves as an etching barrier in this process. Then, patterned etching opens electrode contacts through the thermal SiO_2 layer. Peeling the multilayer structure from the temporary glass substrate yields the final flexible Si-NM MOSFET. More details about the fabrication process can be found in the Supporting Information.

The thermal triggered transient behaviors of Si-NM electronics depend on the properties of the PAMS interlayer. PAMS layer is a high-performance resin widely used in the hollow polymer microsphere for inertial confinement fusion.[24] When heated beyond a certain temperature, the PAMS disaggregates into gaseous monomer. Thermogravimetry (TG) and differential scanning calorimetry (DSC) in Figure 2b reveals thermal decomposition process of PAMS. TG curve shows that the decomposition of PAMS happens in a temperature range (≈250–315 °C). Endothermic peak in DSC curve indicates that PAMS reaches a maximum degradation rate at 285 °C. In this context, the degradation of PAMS involves two stages (Figure S3, Supporting Information).[24] First, random thermal scissions break the polymer chains at weak points and create two kinds of radical chain segments (quaternary carbon radical and primary carbon radical). Second, the radical chain segments depolymerize into monomers or small molecular products.[25] Devices fabricated on PAMS interlayer will be destructed when large amount of volatile products from the second stage gather below the Si-NM functional layer.

2.3. Mechanical Flexibility of the Si-NM Devices with PAMS

The excellent mechanical property of single crystal Si-NM[25–28] provides the flexible and bendable character of the electronic, which dramatically expands the application range in, e.g., narrow space for high-temperature equipment. In order to affirm the compatibility of PAMS in the current flexible device, bending tests were carried out by cyclic curving the device on a glass cylinder (with a radius of 7 mm, inset of **Figure 3**a). Device performance was recorded after 0, 25, 50, 75, and

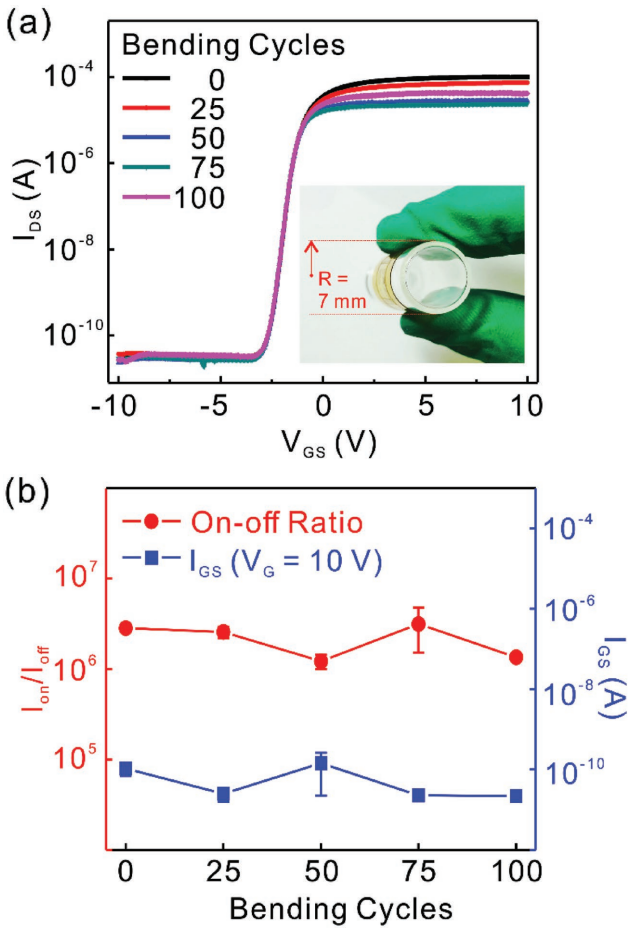

Figure 3. Performance of Si-NM MOSFET under bending test. a) Transfer characteristics of a Si-NM MOSFET in the initial status and after 0 to 100 bending cycles at a step of 25 cycles. The supply voltage is 0.1 V and bending radius is 7 mm. The inset shows the curved Si-NM MOSFET. b) Key parameters of the Si-NM MOSFET in the initial status and after bending test.

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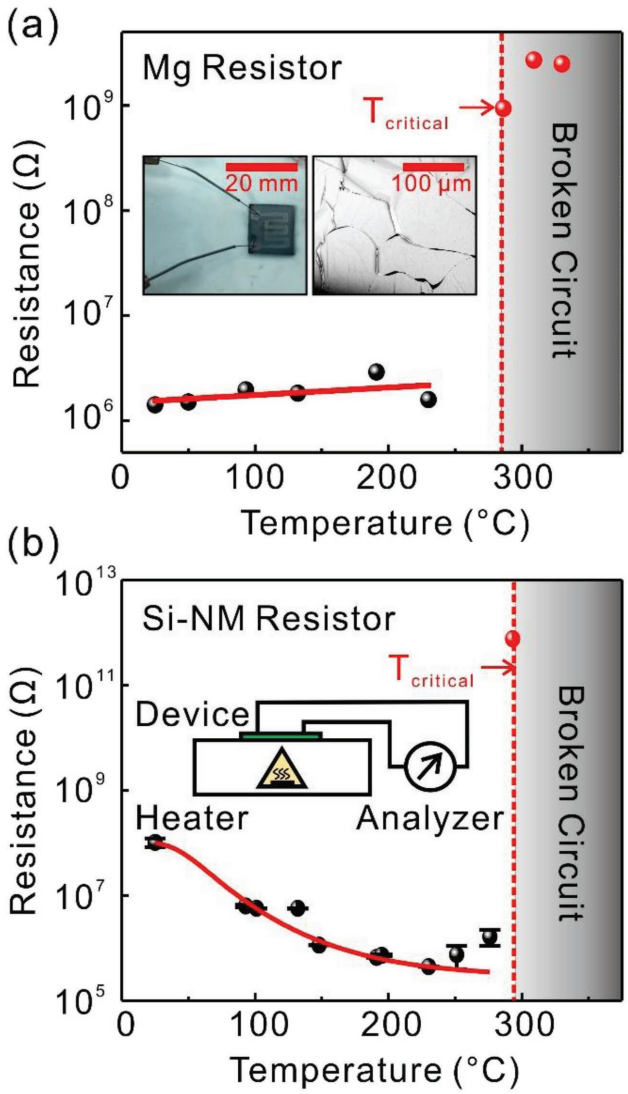

Figure 4. Characterization of thermally triggered transient resistors. a) Real-time characterization of the Mg-resistor at different temperatures. The left inset displays the Mg-resistor on PAMS in real-time characterization. The right inset exhibits the SEM image of the cracked surface of a failed Mg-resistor. b) Real-time characterization of the Si-NM resistor at different temperatures. Inset shows the configuration of the measurement.

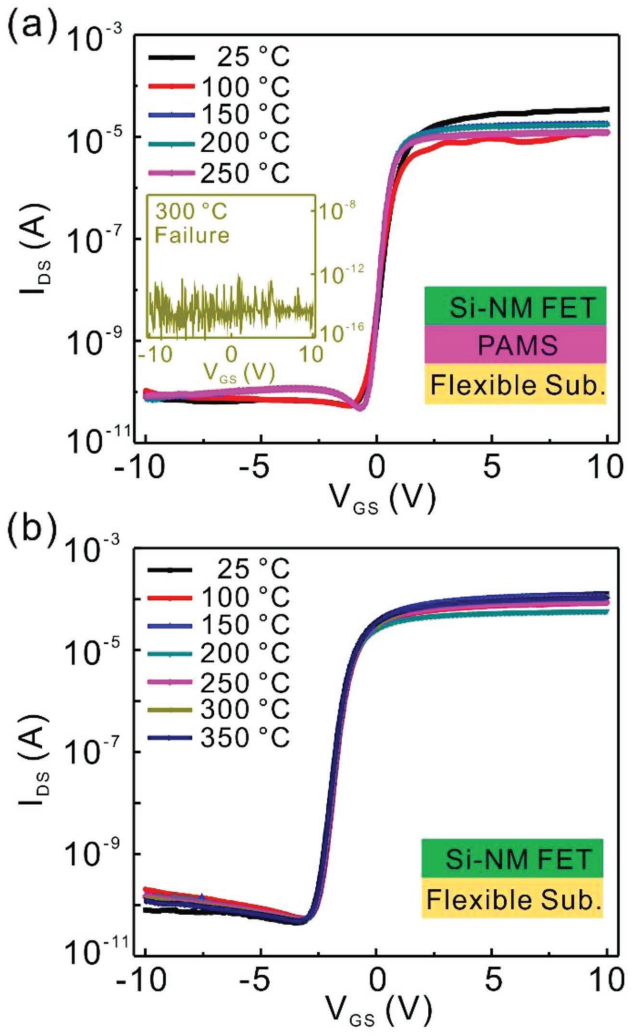

Figure 5. Characterization of thermally triggered transient MOSFET. a) Temperature-dependent transfer characteristics of Si-NM MOSFET on PAMS. The data were collected at room temperature after the device was heated for 3 min. The inset shows the electrical property of the device after being heated to 300 °C for 3 min. b) Temperature-dependent transfer characteristics of a device without PAMS interlayer.

100 bending cycles. Figure 3a shows transfer curves of the FET after certain bending cycles (V_{DS} = 0.1 V). While the high consistency of the curves indicates that the characteristic of the transistor remains stable in the bending tests. Figure 3b presents the statistics regarding on–off ratio and gate leakage current of the device after bending cycles. Both parameters are stable after all these bending tests. We note that interfacial imperfections could reduce the effective mobility while defects in gate oxide would increase gate leakage.[29,30] No obvious functional damage occurs in the device during the bending cycles, which confirms the reliability of current Si-NM MOSFET with PAMS layer integrated in flexible application.

In practice, in the bending state of a brittle film, the maximum strain ε appears on its top surface, which locates farthest way from the neutral surface, and this determines the critical bending radius r_c[31]

$$r_c = \frac{t}{2\varepsilon_{\text{failure}}} \quad (1)$$

where t is the film thickness and $\varepsilon_{\text{failure}}$ is the fracture limits. The $\varepsilon_{\text{failure}}$ is ≈1% for Si and top SiO_2 layers.[21] The total thickness of the Si-NM MOSFET multilayer system is ≈25 μm. Taking the middle layer as the neutral surface for a cursory estimation, the minimum bending radius should be ≈1.25 mm. In this estimation, the substrate was considered as brittle film like silicon. When employing softer polymer substrate in practice, for a given bending radius and substrate thickness, the softer substrate can help to reduce the strain of the device on it.[32] Therefore, the theoretical bending limit of our device could be much smaller than 1.25 mm. In this case, the current FET

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exhibited fine flexibility and reliable functionality in above bending tests.

2.4. Thermally Triggered Transient Resistors

As a proof-of-concept, a Mg (magnesium)-resistor was fabricated and tested on a temperature-controllable environment to demonstrate this thermal triggered destruction process. Temperature-dependent electrical characterization in **Figure 4**a shows the resistance of the Mg resistor maintains at 10^6 Ω with a temperature less than ≈280 °C and increases dramatically to 10^9 Ω at higher temperature. Left inset in Figure 4a displays the photograph of the resistor in this real-time temperature–electrical characterization. Scanning electron microscope (SEM) image (right inset in Figure 4a) of the corresponding heated resistor indicates noticeable structure destruction caused by PAMS decomposition.

Furthermore, the channel resistance of a Si-NM resistor as a function of temperature was investigated by a real-time electrical characterization (Figure 4b), and the inset of Figure 4b shows the configuration of the measurement. At room temperature (RT), the resistance is ≈10^8 Ω. The resistance decreases dramatically with the increasing temperature before ≈250 °C due to the thermally excited carrier.[33] The channel resistance shows a rising trend at ≈250–300 °C, where PAMS starts to degrade (see also Figure 2b). At ≈300 °C, the resistance abruptly increases to 10^{12} Ω, showing the behavior of a broken circuit. The stepwise destruction of the Si-NM resistor is illustrated in Figure S4a in the Supporting Information. Here, the critical failure temperature ($T_{critical}$) of the Si-NM resistor is right higher than the maximum degradation rate temperature (i.e., 285 °C in Figure 4c). This indicates that the device collapses after complete degradation of PAMS, which is consistent with the results shown in Figure 4a. In practice, the thermally triggered transient behavior of the current device happens in a very short time (≈3 min). In the initial stage of the PAMS degradation, thermally triggered scission of polymer chains and a limited amount of volatile products weakened the electronic performance of Si-NM resistor. After the critical failure temperature reached, a large quantity of gas gathered below Si-NM, and the accompanying high pressure led to the breakdown of the device.

2.5. Thermally Triggered Transient MOSFET

Based on the performance of the transient resistors above, we consider that Si-NM MOSFET fabricated on PAMS interlayer could also be destructed upon heated above decomposition temperature. We further investigated the thermal triggered transient behavior of the MOSFET by means of temperature-dependent electrical characterization. The measurements were carried out at room temperature after the device was heated at various designed temperatures for ≈3 min. **Figure 5**a displays the temperature-dependent transfer characteristics of a Si-NM MOSFET on PAMS (the bottom-right inset highlights the structure of the device). The transfer curves indicate the stable gate-controlled ability of FET. The upper-left inset demonstrates that no channel current can be detected after the device was heated to 300 °C, indicating the functional failure of the Si-NM MOSFET when heated beyond $T_{critical}$. The destruction process of Si-MOSFET has been illustrated in Figure S4b in the Supporting Information. For comparison, Figure 5b illustrates the transfer curves of Si-NM MOSFET fabricated by a similar process without PAMS layer. The overlapped curves exhibit the robustness of this Si-NM MOSFET even after heated to 350 °C.

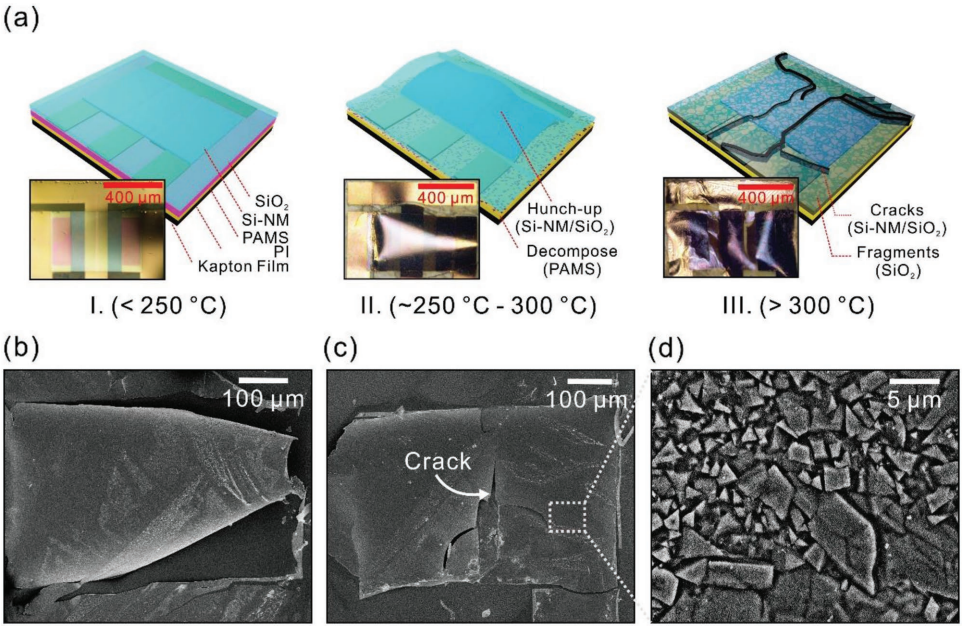

Figure 6. Surface morphologies of the heated device. a) Schematics of the device in the thermally triggered failure process. SEM images of the failed device: significant bending of b) device layer and c) cracks on the device. d) SEM image at high magnification shows fragmental surface, indicating an irreversible destruction of the device.

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The thermal stability of both devices (Figure 5a,b) proves good high-temperature endurance of the flexible device, while the device failure (Figure 5a) at elevated temperature confirms the thermal triggered transient process due to thermal decomposition of PAMS.

2.6. Failure Model

We investigated the transient process by using the detailed morphological characterization. **Figure 6**a schematically illustrates typical steps of the transient process. The corresponding insets below display the optical microscopy images of Si-NM MOSFET in individual steps. The as-fabricated device in Figure 6a-(I) shows the initially smooth surface, accompanied with good transistor characteristics below 250 °C. When heated to ≈250–300 °C, the PAMS layer starts to decompose and releases volatile monomers. Pressure from gas products leads to the deformation of the Si-NM device layer. The hunched device (Figure 6a-(II)) leads to functional degradation, as shown in Figure 4b. At even high temperature (i.e., >300 °C), continuous collection of volatile products below device layer yields local high pressure in a short time. Consequently, device layer breaks into small and separate parts with cracks, as shown in Figure 6a-(III). Such fragmentation process typically takes place in thin film in order to release deformation energy,[34] and more experimental observations are exhibited in Figure 6b–d. SEM images in Figure 6b,c exhibit two typical failure models. Significant bending of the device layer is noticeable. Figure 6c also demonstrates that cracks may form in the deformed device layer. Enlarged SEM image in Figure 6d shows that the device layer is actually broken into even smaller pieces in the transient process, indicating the stress in the device layer produced by the underneath gaseous products has exceeded the ultimate tensile strength (UTS). Elemental analysis (Figure S5, Supporting Information) proves that metal contact is still intact while Si/SiO_2 layer is broken. This indicates that the SiO_2 encapsulation layer is easy to fragment in the failure process, which causes that destruction of the whole Si-NM MOSFET.

In order to confirm this failure model theoretically, finite element analysis (FEA) was used to study the strain/stress in a SiO_2/Si (340 nm/ 2 µm) bilayer on pressurized gas. **Figure 7**a illustrates the simplified model of Si-NM device in the FEA analysis (see Supporting Information for details). For thermal SiO_2 layer, UTS is 110 MPa,[35] and SiO_2 encapsulation layer should be fractured if the Von Mises stress exceeds this value. The total displacement and distribution of stress in SiO_2 layer with the maximum value just below UTS (the critical state) is shown in Figure 7b,c, where the corresponding pressure of the gas is ≈23 kPa. At this state, the device arched upward with a maximum displacement of 11.89 µm. The arched distortion in FEA simulation corresponds to the phenomenon in experiment. In our device, the maximum gas pressure at 300 °C was estimated to be 43.31 MPa (see Supporting Information for details), indicating the device on Si-NM can be easily destroyed by the gas in this circumstance, as experimentally observed in Figure 6. Further theoretical investigation demonstrates that the device on Si-NM with thickness even up to micrometer can be easily destroyed in a similar process.

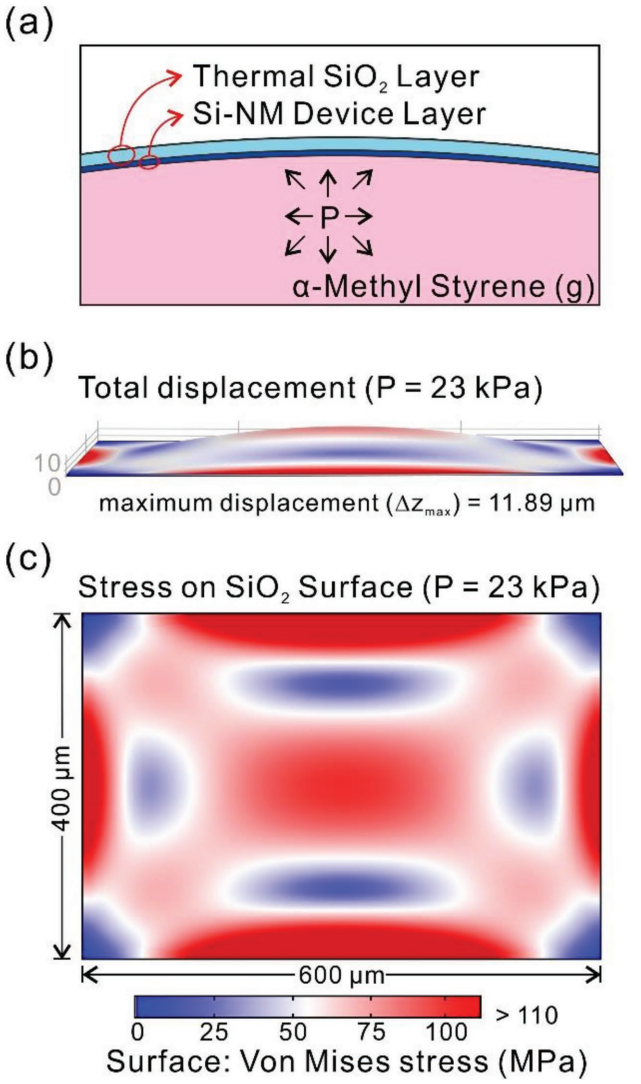

Figure 7. FEA analysis of the device under the pressure load of PAMS degradation products. a) Schematic illustration of the model in FEA simulation; b) Total displacement of the device at the critical state (gas pressure $P = 23$ kPa); c) Stress distribution on thermal SiO_2 layer surface at the critical state.

3. Conclusion

We reported materials, designs, and fabrication strategy that involve thermal degradable PAMS to fabricate transient devices which can operate properly at high temperature (<250 °C). Such adaptability mainly benefits from the decomposition behavior of PAMS and thermal stability of flexible substrate as well as the ultrathin device structure. Basic electrical measurements and bending tests confirm that the integration of PAMS interlayer has no influence on the device performance and flexibility. A comprehensive assessment reveals that when triggered by high temperature (>300 °C), products of PAMS degradation cause distortion of the Si-NM functional layer and finally result in an irreversible destruction of the device in the form of structure fragmentation. This work provides a foundation for understanding the transient mode for future on-chip components in

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high-temperature electronic applications, such as circuit safeguard, privacy protection, sensing, and control devices, etc. We expect that more thermal degradable materials can be engaged for flexible transient devices for various application scenarios.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

high-temperature-triggered degradation, poly-α-methylstyrene, silicon nanomembranes, transient electronics

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[1] K. K. Fu, Z. Wang, J. Dai, M. Carter, L. Hu, *Chem. Mater.* **2016**, *28*, 3527.
[2] J. K. Chang, H. Fang, C. A. Bower, E. Song, X. Yu, J. A. Rogers, *Proc. Natl. Acad. Sci. USA* **2017**, *114*, E5522.
[3] S.-W. Hwang, H. Tao, D.-H. Kim, H. Cheng, J.-K. Song, H. Tao, D.-H. Kim, H. Cheng, J.-K. Song, E. Rill, M. A. Brenckle, B. Panilaitis, S. M. Won, Y.-S. Kim, Y. M. Song, K. J. Yu, A. Ameen, R. Li, Y. Su, M. Yang, D. L. Kaplan, M. R. Zakin, M. J. Slepian, Y. Huang, F. G. Omenetto, J. A. Rogers, *Science* **2012**, *28*, 1640.
[4] Y. Gao, Y. Zhang, X. Wang, K. Sim, J. Liu, J. Chen, X. Feng, H. Xu, C. Yu, *Sci. Adv.* **2017**, *3*, e1701222.
[5] S. K. Kang, S. W. Hwang, H. Y. Cheng, S. Yu, B. H. Kim, J. H. Kim, Y. G. Huang, J. A. Rogers, *Adv. Funct. Mater.* **2014**, *24*, 4427.
[6] S. K. Kang, R. K. J. Murphy, S. W. Hwang, S. M. Lee, D. V. Harburg, N. A. Krueger, J. H. Shin, P. Gamble, H. Y. Cheng, S. Yu, Z. J. Liu, J. G. McCall, M. Stephen, H. Z. Ying, J. Kim, G. Park, R. C. Webb, C. H. Lee, S. J. Chung, D. S. Wie, A. D. Gujar, B. Vemulapalli, A. H. Kim, K. M. Lee, J. J. Cheng, Y. G. Huang, S. H. Lee, P. V. Braun, W. Z. Ray, J. A. Rogers, *Nature* **2016**, *530*, 71.
[7] C. H. Lee, J.-W. Jeong, Y. Liu, Y. Zhang, Y. Shi, S.-K. Kang, J. Kim, J. S. Kim, N. Y. Lee, B. H. Kim, K.-I. Jang, L. Yin, M. K. Kim, A. Banks, U. Paik, Y. Huang, J. A. Rogers, *Adv. Funct. Mater.* **2015**, *25*, 1338.
[8] H. L. Hernandez, S. K. Kang, O. P. Lee, S. W. Hwang, J. A. Kaitz, B. Inci, C. W. Park, S. Chung, N. R. Sottos, J. S. Moore, J. A. Rogers, S. R. White, *Adv. Mater.* **2014**, *26*, 7637.
[9] B. H. Kim, J.-H. Kim, L. Persano, S.-W. Hwang, S. Lee, J. Lee, Y. Yu, Y. Kang, S. M. Won, J. Koo, Y. K. Cho, G. Hur, A. Banks, J.-K. Song, P. Won, Y. M. Song, K.-I. Jang, D. Kang, C. H. Lee, D. Pisignano, J. A. Rogers, *Adv. Funct. Mater.* **2017**, *27*, 1606008.
[10] Y. Gao, K. Sim, X. Yan, J. Jiang, J. Xie, C. Yu, *Sci. Rep.* **2017**, *7*, 947.
[11] A. Gumus, A. Alam, A. M. Hussain, K. Mishra, I. Wicaksono, G. A. Torres Sevilla, S. F. Shaikh, M. Diaz, S. Velling, M. T. Ghoneim, S. M. Ahmed, M. M. Hussain, *Adv. Mater. Technol.* **2017**, *2*, 1600264.
[12] J. Lee, B. Yoo, H. Lee, G. D. Cha, H.-S. Lee, Y. Cho, S. Y. Kim, H. Seo, W. Lee, D. Son, M. Kang, H. M. Kim, Y. I. Park, T. Hyeon, D.-H. Kim, *Adv. Mater.* **2017**, *29*, 1603169.
[13] Y. H. Jung, T. H. Chang, H. L. Zhang, C. H. Yao, Q. F. Zheng, V. W. Yang, H. Y. Mi, M. Kim, S. J. Cho, D. W. Park, H. Jiang, J. Lee, Y. J. Qiu, W. D. Zhou, Z. Y. Cai, S. Q. Gong, Z. Q. Ma, *Nat. Commun.* **2015**, *6*, 7170.
[14] M. A. Huque, S. K. Islam, L. M. Tolbert, B. J. Blalock, *IEEE Trans. Power Electron.* **2012**, *27*, 4153.
[15] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, Z. Liang, D. Costinett, B. J. Blalock, *IEEE Trans. Power Electron.* **2015**, *30*, 1432.
[16] A. M. Hussain, M. M. Hussain, *Adv. Mater.* **2016**, *28*, 4219.
[17] J. A. Rogers, M. G. Lagally, R. G. Nuzzo, *Nature* **2011**, *477*, 45.
[18] C. Y. Li, F. E. Sauser, R. G. Azizkhan, C. H. Ahn, I. Papautsky, *J. Micromech. Microeng.* **2005**, *15*, 1729.
[19] R. Torrance, T. Viswanathan, J. V. Hanson, *IEEE Trans. Circuits Syst.* **1985**, *32*, 1097.
[20] D. K. Schroder, *Semiconductor Material and Device Characterization*, John Wiley & Sons, Hoboken, NJ **2006**.
[21] H. Fang, K. J. Yu, C. Gloschat, Z. Yang, C. H. Chiang, J. Zhao, S. M. Won, S. Xu, M. Trumpis, Y. Zhong, E. Song, S. W. Han, Y. Xue, D. Xu, G. Cauwenberghs, M. Kay, Y. Huang, J. Viventi, I. R. Efimov, J. A. Rogers, *Nat. Biomed. Eng.* **2017**, *1*, 1.
[22] B. Zhu, H. Wang, W. R. Leow, Y. Cai, X. J. Loh, M. Y. Han, X. Chen, *Adv. Mater.* **2016**, *28*, 4250.
[23] E. M. Song, H. Fang, X. Jin, J. Zhao, C. Jiang, K. J. Yu, Y. Zhong, D. Xu, J. Li, G. Fang, H. Du, J. Zhang, J. M. Park, Y. Huang, M. A. Alam, Y. F. Mei, J. A. Rogers, *Adv. Electrode Mater.* **2017**, *3*, 1700077.
[24] B. W. McQuillan, A. Nikroo, D. A. Steinman, F. H. Elsner, D. G. Czechowicz, M. L. Hoppe, M. Sixtus, W. J. Miller, *Fusion Technol.* **1997**, *31*, 381.
[25] S. L. Malhotra, C. Baillet, L. Minh, L. P. Blanchard, *J. Macromol. Sci., Part A: Pure Appl. Chem.* **1978**, *A12*, 129.
[26] G. S. Huang, Y. F. Mei, *Small* **2018**, *14*, 1703665.
[27] E. M. Song, Q. L. Guo, G. S. Huang, B. Jia, Y. F. Mei, *ACS Appl. Mater. Interfaces* **2017**, *9*, 12171.
[28] Q. L. Guo, M. Zhang, Z. Y. Xue, G. Wang, D. Chen, R. G. Cao, G. S. Huang, Y. F. Mei, Z. F. Di, X. Wang, *Small* **2015**, *11*, 4140.
[29] M. Asadirad, S. Pouladi, S. Shervin, S. K. Oh, K. H. Lee, J. Kim, S.-N. Lee, Y. Gao, P. Dutta, V. Selvamanickam, J.-H. Ryou, *IEEE Electron Device Lett.* **2017**, *38*, 217.
[30] L. Yan, H. B. Lu, G. T. Tan, F. Chen, Y. L. Zhou, G. Z. Yang, W. Liu, Z. H. Chen, *Appl. Phys. A: Mater. Sci. Process.* **2003**, *77*, 721.
[31] J. A. Rogers, J.-H. Ahn, *Silicon Nanomembranes: Fundamental Science and Applications*, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, Germany **2016**.
[32] T. Das, X. Chen, H. Jang, I. K. Oh, H. J. Kim, J. H. Ahn, *Small* **2016**, *12*, 5720.
[33] P. P. Altermatt, A. Schenk, F. Geelhaar, G. Heiser, *J. Appl. Phys.* **2003**, *93*, 1598.
[34] Z. Qin, N. M. Pugno, M. J. Buehler, *Sci. Rep.* **2014**, *4*, 4966.
[35] http://www.mit.edu/~6.777/matprops/sio2.htm, (accessed: February **2018**).

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