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Nanogranular SiO_2 proton gated silicon layer transistor mimicking biological synapses

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Silicon on insulator (SOI)-based transistors gated by nanogranular SiO_2 proton conducting electrolytes were fabricated to mimic synapse behaviors. This SOI-based device has both top proton gate and bottom buried oxide gate. Electrical transfer properties of top proton gate show hysteresis curves different from those of bottom gate, and therefore, excitatory post-synaptic current and paired pulse facilitation (PPF) behavior of biological synapses are mimicked. Moreover, we noticed that PPF index can be effectively tuned by the spike interval applied on the top proton gate. Synaptic behaviors and functions, like short-term memory, and its properties are also experimentally demonstrated in our device. Such SOI-based electronic synapses are promising for building neuromorphic systems. *Published by AIP Publishing.*
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In neural systems, through a synapse, a potential spike signal from a presynaptic neuron can trigger an ionic excitatory postsynaptic current (EPSC) that lasts for 1–10^4 ms in a postsynaptic neuron. Signal processing, memory and learning functions of the brain are realized through such ionic fluxes between the neurons and synapses. During this process, ions and protons are the key medium of neural transportation. Experiments on animals' synapse shows that synaptic modifications can be adjusted by the concentrations of ionic species.[1] It should be remarked that some studies, concerning possibilities of electronic model of signal processing in nervous systems, take into account wide spectrum of neurophysiological phenomena, including synapse short-distance and long-distance communication and dendro-dendritic coupling.[2] The change by the history of neuron activity could be either enhancement or depression. It is believed that such activity-dependent synaptic plasticity is in charge of memory and learning of the brain. The electrical devices that simulate and analyse EPSC signal for neural system can be an important way to the study of neural electronics. For instance, a two-terminal device realizing EPSC signal has been fabricated by multi-quantum-dot,[3] and a $Ta/TaO_x/TiO_2/Ti$ device was recently fabricated with great potential of implementing high-density crossbar memory arrays with numerous highly desirable features.[4] However, the complicated fabrication process and circuit design may constrain its practical application. Another option for mimicking neural systems is the ionic materials. Brain behaviors like short term memory (STM) are mimicked by ionic conductor.[5] For field effect transistors (FETs), ionic/electronic hybrid devices gated by ion conducting electrolytes, the migration of ions can modulate the carrier transport characteristics of channel layer by forming the electric double layer (EDL).[6,7] The EDL formed by ionic liquids has become a promising approach of scientific research on electrostatic surface charge.[8] Gate dielectrics formed by ionic liquids are demonstrated to achieve an electrostatic surface charge accumulation on the order of $10^{14}\,cm^{-2}$.[9,10] With huge charge accumulation at the gate/channel surface, it takes more time to accumulate and relax the ions in ionic gate materials. For the industry application of integrated EDL transistors, a solid ion gate is obviously a better choice than the expensive ionic liquid gates. By using solid proton conductors, researches have shown that in-plane lateral-coupled oxide-based artificial synapse network coupled by protons can be self-assembled on glass substrates at room-temperature, and a strong lateral modulation is observed on the device due to the proton-related EDL effect.[11] As is known to all, silicon remains the most common-used channel material in the integrated circuits. FET sensors based on silicon substrate or SiO_2/silicon substrate have gained much attention due to their reliability and reproducibility fabrication process.[12,13] Especially, the silicon-on-insulator (SOI) is widely used in opto-electronics, microelectronics, and nanoelectromechanical systems and has become the platform for future high-speed electronic devices.[14–16] SOI has the advantage of better latch up immunity, reduced junction capacitance, higher drive current, ease of making shallow junctions compares, and lower short channel effects.[17–19] Silicon nanomembranes (SiNMs) from SOI even have demonstrated the potential in flexible and wearable electronics.[20] For extra p-dope and n-dope of SiNM on SOI, transistors based on ionic/electronic hybrid materials by integrating a layer of ionic conductor and a layer of ion-doped conjugated polymer can be integrated in large-scale circuits for the emulations of brain functions.[21]

In this work, we developed a facile process of fabricating nanogranular SiO_2 proton gate on near-instinct P-type SOI. Because of the high planar capacitance of nanogranular SiO_2 proton and the surface effect on top of the Si layer, our device mimicked the EPSC properly. Synaptic behaviors and

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functions, such as paired-pulse facilitation (PPF) and STM, are experimentally demonstrated. Combining SOI with nanogranular SiO_2 proton gate could be promising in building neural mimicking systems with easy and large-area fabrication process.

Figures 1(a) and 1(b) are the schematic diagram and microscope image of SiO_2 proton transistors on SOI, respectively. We made Cr/Au (10 nm/100 nm) electrode pads on 50-nm-thick Si layer (top Si layer of the SOI substrate) by photolithography and magnetron sputtering. Then, rapid thermal process (300 °C, 30 s) was applied in N_2 atmosphere to obtain better electrical contacts. After that, we used plasma-enhanced chemical vapor deposition (PECVD) to grow ~500 nm thick nanogranular SiO_2 proton conductor as the top gate (TG) at room temperature. And then water molecules can be absorbed from the air. High proton conductivity nanogranular SiO_2 is considered to be due to the sequence of proton hopping between hydroxyl groups and water molecules under applied electric field.[11,22] More details of fabrication process and the nanogranular structure can be found in our previous work.[11] Finally, Au pads with the thickness of 50 nm were sputtered as top gate (TG) electrode. Given that the bulk silicon in the bottom of SOI can be regarded as another gate electrode (back gate, BG), there are two gates in our transistor. Figure 1(c) illustrates the output curve when the voltage was applied on the TG (nanogranular SiO_2 proton gate) and the I_{DS}-V_{DS} curves are typical for FET. From Fig. 1(c), one can see that the current of our transistor reaches one order of magnitude larger when TG voltage changes from 4 to −3 V for near-intrinsic p-type Si channel layer.

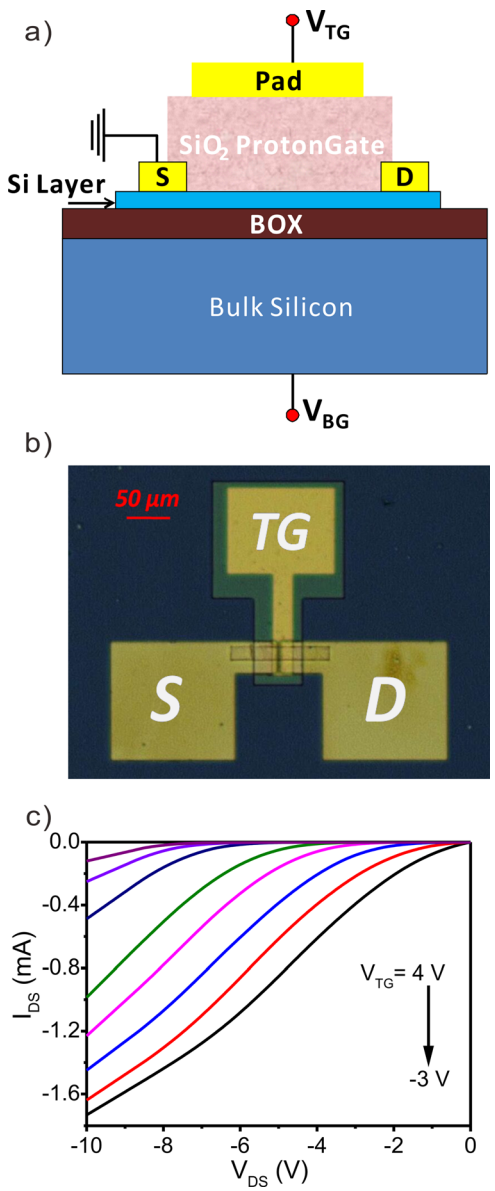

FIG. 1. (a) Schematic diagram of SOI/SiO_2 transistors gated by nanogranular SiO_2 proton conducting electrolytes. We used photolithography to pattern SiNMs (light blue part) on SOI. After fabricating the Au pad electrodes, PECVD was used to grow ~500 nm nanogranular SiO_2 proton as top gate (pink region) at room temperature. (b) Optical microscope image of the devices. The gap between source and drain is 5 μm. (c) I_{DS}–V_{DS} curves with different TG voltages (V_{TG}, step: 1 V).

Figures 2(a) and 2(b) show transfer curve at different gate voltages (V_{TG} and V_{BG}, respectively) under constant $V_{DS} = 1$ V. Due to the distributions of protons in SiO_2 electrolyte layer,[23] an electrical hysteresis curve can be seen in Fig. 2(a). With increasing V_{TG} (i.e., from negative to positive, Fig. 2(a)), H^+ are accumulated to the TG pad and OH^- left inside the SiO_2 EDL gate will induce holes in the Si channel, causing an I_{DS} higher than that in the back loop. With the decrease in V_{TG} (i.e., from positive to negative), the accumulated protons (e.g., H^+) are not diffused at once which needs micro-seconds to get to the initial state, and the density of holes in the channel are decreased due to the high density of H^+ in the SiO_2 EDL gate, causing a depletion of carriers, which explains the lower I_{DS}. Thus, the hysteresis phenomenon can be observed. Contrarily, for normal BG, there is no electrical hysteresis behavior, as shown in Fig. 2(b). This is reasonable since no mobile proton exists in BG. Figure 2(c) shows the I_{DS} as a function of V_{TG} with different V_{DS}. We can see that the turning point of the electrical hysteresis curve changes under different V_{DS}: the higher V_{DS},

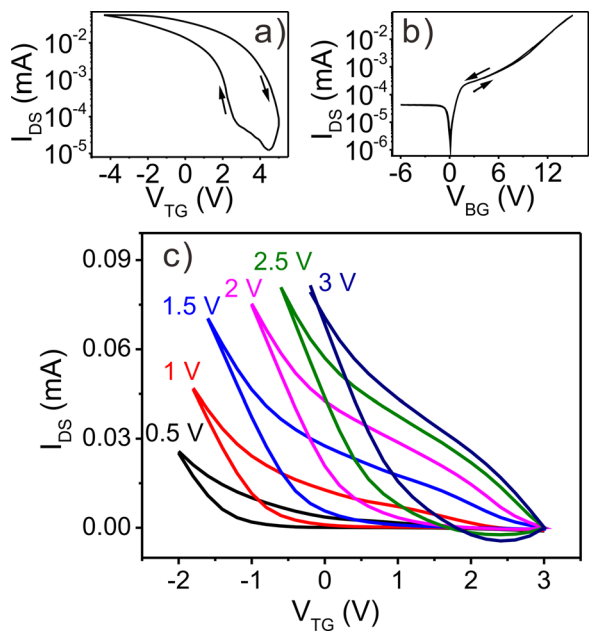

FIG. 2. (a) Transfer curve I_{DS}–V_{TG} with constant $V_{DS} = 1$ V when the gate voltage was applied on TG. (b) Transfer curve I_{DS}–V_{BG} with constant $V_{DS} = 1$ V when the gate voltage was applied on the bulk silicon (BG). (c) Transfer curves I_{DS}–V_{TG} with different V_{DS}.

the higher turning point. The area of the loop increases when the V_{DS} gets larger, indicating that there is a larger internal planar electric field when the drain voltage is applied. The drain voltage and corresponding internal planar electric field will cause the redistribution of the H^+ at the surface near the source and drain (i.e., holes at the surface between proton gate/Si channel). When the drain voltage is positive, there will be more protons near drain in proton gate right above the Si channel, which cause more time to accumulate holes if the holes are not averagely placed at the surface. The higher drain voltage is, the more time it takes to accumulate the proton, which cause the large area of the loop.

When a presynaptic spike is applied on the pre-synapse, H^+ in SiO_2 layer will migrate to the SiO_2/Si layer interface in Si channel to trigger an EPSC, as shown in Fig. 3(a). Typical EPSCs was triggered by two successive presynaptic spikes (2 V) with intervals of 10 and 100 ms (upper and lower panels in Fig. 3(a), respectively. Time resolution: 10 ms). The amplitude of EPSC triggered by the second presynaptic spike is 1.23 times larger than that triggered by the first spike when the interval is 10 ms (upper panel). Here, we define paired pulse facilitation (PPF) index (i.e., increase ratio) as $(A_1 - A_0)/A_0$. To investigate the influence of the second pulse voltage applied on the top nanogranular SiO_2 proton gate to PPF of the synaptic transistor, a series of successive pulse of different interval times (10, 20, 30, 40, 50, and 100 ms) were applied on the gate. Figure 3(b) shows the change of increase in ratio as a function of different interval time. The magnitude of PPF index decreases as the pulse interval time increases. The PPF index reaches a maximum value of ~22.9% when interval time is 10 ms and it decreases to near 10% when the pulse interval is long enough (e.g., 100 ms). Here, we found that the magnitude of index decreases sharply when the interval time is small while the decrease in index at longer interval time is slow, which can be fitted by an exponential curve (Fig. 3(b)). This is because the migration of protons in the nanogranular SiO_2 layer plays an important role for EPSC triggering, and the increase in channel current is due to the proton migration and interfacial EDL electrostatic modulation.[24] When the interval time is short, the protons triggered by the first spike still partially accumulate at the interface of the nanogranular SiO_2 layer/Si channel when the second spike comes. The total amount of the accumulated protons will get larger due to the integrated effect. While for long interval time, the protons triggered by the first spike will diffuse back to the equilibrium position, causing the summation effect to disappear and the PPF index to decrease.[11] In Fig. 3(b), the inset shows the EPSCs triggered by two successive presynaptic spikes with spike interval of 10 ms at different V_{DS}. The increase in EPSC with increasing V_{DS} is obvious: when we change the V_{DS} from 1 to 2 V, the EPSC signal changes by one order of magnitude. However, if V_{DS} is increased to 3 V (not shown), the EPSC signal becomes disordered due to the leak current as can be seen from Fig. 2(c). After positive gate pulse, a period of time is required for the interfacial protons to diffuse back to their equilibrium position. The EPSCs will gradually reduce to the initial value in several micro-seconds. This time is a reflection of proton release, also called "relaxation time." As is known to all, the EPSC response of presynapse plays an important role in neuron systems. We have measured related EPSC response at different amplitudes of successive presynapse (pulse width: 10 ms; interval time: 10 ms). A larger presynapse will trigger a stronger EPSC signal: larger I_{DS} and longer relaxation time, which results in a larger PPF because the 2nd EPSC signal will surely be larger than the 1st signal and more protons are accumulated at a larger presynapse voltage (i.e., V_{TG}), as shown in Fig. 3(c).

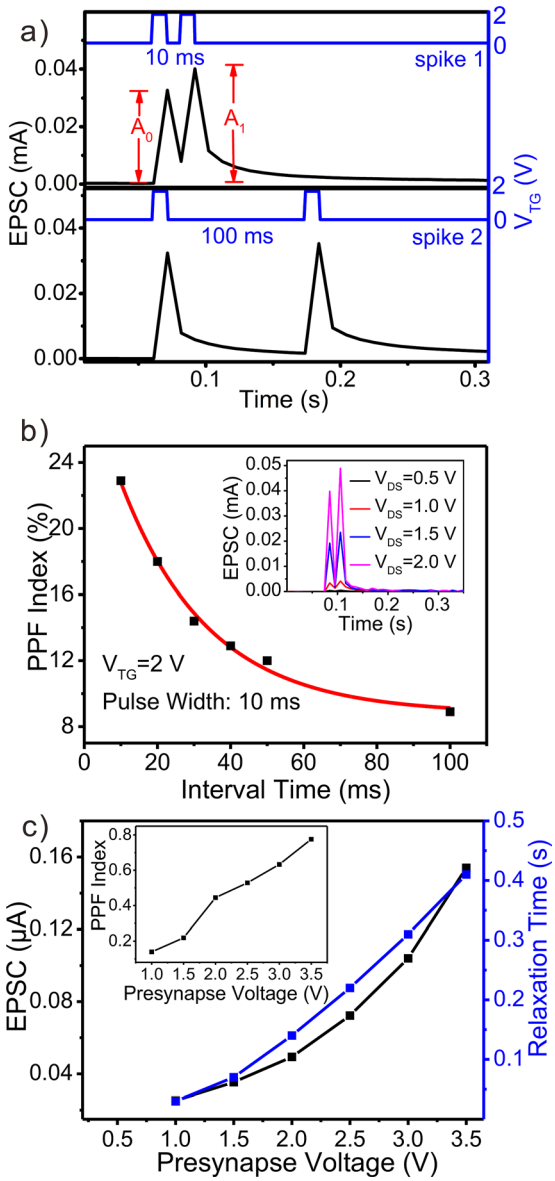

FIG. 3. (a) EPSCs triggered by two successive presynaptic spikes when successive pulse of different interval times (10 and 100 ms) were applied on the gate with $V_{DS} = 2$ V. Here we define the PPF index as $(A_1 - A_0)/A_0$. The time resolution for EPSC measurements is 10 ms. (b) PPF index measured at different interval time. The red line is the exponentially fitting result. The inset shows EPSCs triggered by two successive presynaptic spikes at different V_{DS}. (c) EPSC responses to successive presynapse with different voltages (pulse width: 10 ms; interval time: 10 ms). PPF index as a function of presynapse voltage is shown in the inset.

We also noticed that the intensity of EPSCs increases when a series of pulse were input. The time-dependent channel EPSC behaviors can be regarded as a memory behavior. PPF is thus a form of short-term synaptic plasticity associated with short-term adaptations to sensory inputs, and short-lasting forms of memory.[25] Figure 4(a) shows the EPSC

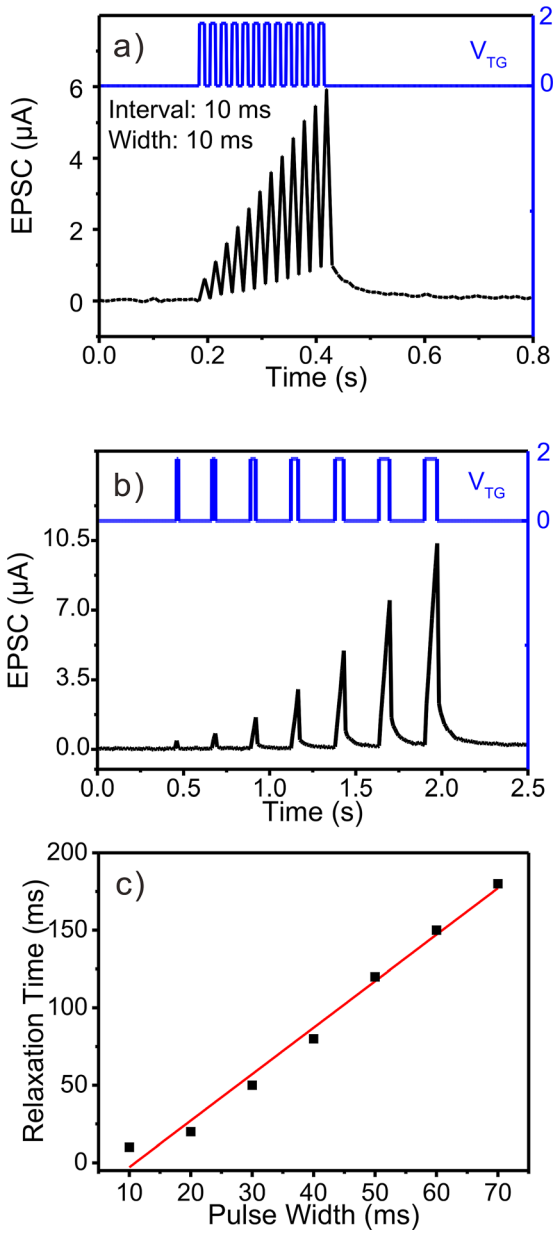

FIG. 4. (a) EPSC responses of the device to stimulus train with a 12 gate spikes (2.0 V, 10 ms). The V_{DS} is fixed at 1 V. (b) The width of the presynapse spike on the gate electrode was changed from 10 to 70 ms. (c) EPSC relaxation time as a function of input pulse width. The black squares are experimental results. The red line is the relaxation time behavior fitted by the linear function.

responses of our device to the stimulus train with 12 gate spikes (2.0 V, 10 ms). The interval time between two pulses is 10 ms, and V_{DS} is set at 1.0 V to measure the channel current. The retention time of the STM state is dependent on a history of the previous input pulse.[11] An obvious enhancement in channel current is observed after each gate pulse and a total current enhancement of ~830% is obtained after eleven gate pulses. This is because more and more protons are accumulated at the electrolyte/Si channel interface when the number of gate pulses increases. After all spikes, the EPSCs will gradually reduce to the initial value.[26] To further study the effect of stimulation rate on the memory behaviors of the transistor, the width of the presynaptic spike on the gate electrode was changed from 10 to 70 ms as shown in Fig. 4(b). When the stimulation pulse width is increased, an obvious enhancement in I_{DS} is observed. Fig. 4(c) shows the EPSC relaxation time with different input pulse width. We can see that the EPSC relaxation time increases with pulse width linearly. At a larger spike width, the process of increasing relaxation time can be regarded as a proper way of turning STM to long term memory (LTM).[27]

In summary, SOI-based EDL transistors gated by proton SiO_2 electrolyte were fabricated at room temperature and artificial synapses based on these devices were carefully investigated. Spikes on proton SiO_2 gate and current I_{DS} could be regarded as presynapse and postsynapse signals, respectively. Presynaptic spikes with duration time-dependent EPSCs were observed in such synaptic transistors. H^+ migration triggered by the gate pulse resulted in the establishments of the inter-coupling between the gate and the Si channel. PPF and STM are experimentally mimicked in such SOI-based synaptic transistors. The results obtained in this work might pave the way for building neuromorphic systems using widely used SOI.

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