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Giant Persistent Photoconductivity in Rough Silicon Nanomembranes

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ABSTRACT

This paper reports the observation of giant persistent photoconductivity from rough Si nanomembranes. When exposed to light, the current in p-type Si nanomembranes is enhanced by roughly 3 orders of magnitude in comparison with that in the dark and can persist for days at a high conductive state after the light is switched off. An applied gate voltage can tune the persistent photocurrent and accelerate the response to light. By analyzing the band structure of the devices and the surfaces through various coatings, we attribute the observed effect to hole-localized regions in Si nanomembranes due to the rough surfaces, where light can activate the confined holes.

Since the beginning, it has been noted that the surfaces of nanomaterials hold great potential for applications.[1−5] In other words, nanomaterial properties can be significantly influenced or manipulated by surface modification.[6−10] For example, through functionalizing Si nanowire surfaces, sensitive and selective detection of biological and chemical species has been realized.[6] By intentionally roughening surfaces, the thermoelectric performance of Si nanowires was greatly enhanced due to the introduction of phonon-scattering elements at several length scales.[7] Very recently, nanomembranes from top-down have attracted increased attention in applications like flexible electronics[11−14] in which it has been found that carrier transport through thin Si nanomembranes is highly affected by the interaction of their surfaces with bulk dopants.[15] Therefore, it is promising that surface modification could offer a versatile and intriguing way to further explore the properties of nanomaterials and improve their performance in potential devices.[6−14] However, there are only few works on photoconductivity of Si nanostructures with modified surfaces[16] although it has been found that such an effect is sensitive to the diameters of nanotubes or nanowires.[17,18]

Persistent photoconductivity (PPC), which means that photoconductivity persists after the illumination has ceased, implies interesting applications in e.g. bistable optical switches[19,20] and radiation detectors;[21,22] it has been primarily observed in compound semiconductors[23−26] and layered structures.[27−29] In contrast, the PPC effect is much weaker in Si. PPC of several times larger magnitude than the dark conductivity is obtained in sulfur-diffused or porous Si.[30,31] In commercially available Si wafers, a specific test structure is required to detect a very weak PPC effect.[32]

In this letter we show that by introducing rough surfaces giant PPC in Si nanomembranes can be achieved at room temperature, which is approximately 3 orders of magnitude larger than the dark conductivity and can persist for a long time (on the order of days) after the light is switched off. Such a PPC effect only happens when holes are injected into the rough Si channel because the suppression of hole transport in the dark is released upon illumination. Interestingly, gate voltages can tune the persistent photocurrent and accelerate the response to light, which can be speeded up by an intense illumination as well. The PPC effect is also obtained in rough Si nanomembranes after various surface coatings via atomic layer deposition (ALD). We thus conclude that rough surfaces can produce hole-localized regions in Si nanomembranes; and the confined holes can be activated by illumination for the observed PPC effect.

Two types of Si nanomembranes were fabricated in the experiments, rough surface samples obtained by a slight wet-chemical etching and smooth surface samples without wet-chemical treatment. Both Si nanomembranes were fabricated from silicon-on-insulator (SOI) wafers with Si/SiO_2 thickness of 27/100 nm (from SOITEC Inc.) and electrically investigated using thin-film transistor structures (Figure 1a). The top Si layer is doped with boron and has a resistivity of about 10 Ω·cm. To pattern the Si nanomembranes and create rough surfaces, wet-chemical etching was used (steps, I−K and II−K in Figure 1a); for comparison, patterned Si nanomembranes with originally smooth surfaces were obtained by reactive ion etching masked with photoresist (steps, I-R and II-R in Figure 1a). During the process to form rough Si

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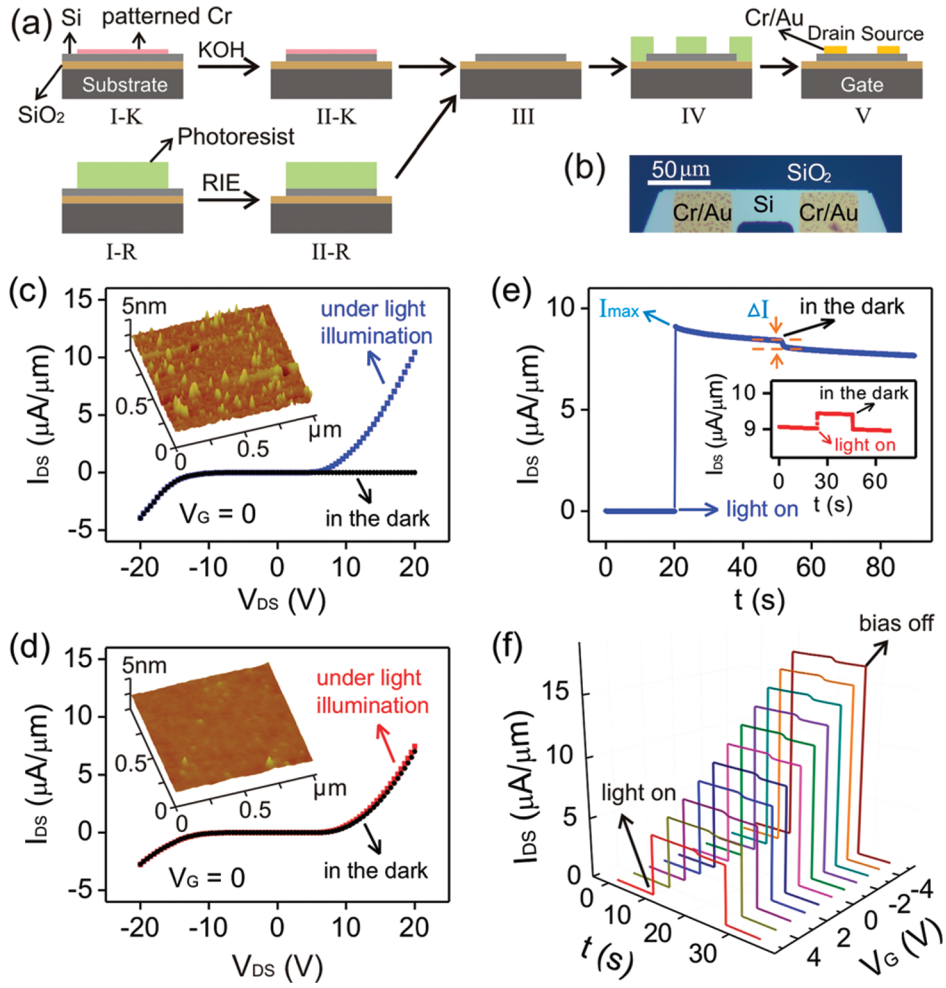

Figure 1. (a) Schematic of the Si nanomembrane roughening and the processing flow for the corresponding devices. Patterned Cr masks (I−K) were used for KOH wet etching (II−K) to create rough surfaces. For comparison, photoresist masks (I-R) were used for reactive ion etching (II-R) to preserve the original smooth surfaces. Both types of Si nanomembranes (III) were patterned by photoresist (IV) to define the drain and source electrodes (V). (b) Optical microscopy image of a representative fabricated device. (c) $I_{DS}-V_{DS}$ properties of the rough Si nanomembrane in the dark and under light illumination. Inset: AFM image of a rough Si nanomembrane. (d) $I_{DS}-V_{DS}$ properties of the smooth Si nanomembrane in the dark and under light illumination. Inset: AFM image of the original smooth Si nanomembrane. (e) Typical PPC results at $V_{DS} = 20$ V and $V_G = 2$ V. The inset shows the "normal" photoresponse of a smooth Si nanomembrane. (f) PPC results at $V_{DS} = 20$ V, measured at different gate voltages; from left to right, V_G decreases from 5 to −5 V at steps of 1 V.

surfaces, 10 nm thick Cr masks deposited by electron beam evaporation were used to pattern the wafer (I−K). After rinsing in 5 wt % HF for 30 s to remove the native oxide, the Cr-film-patterned SOI wafer was immersed into 20 wt % KOH aqueous solution at 50 °C for 35 s (II−K). During the process, the etching solution could penetrate through the thin Cr masks and etch the underlying Si nanomembranes slightly, producing rough surfaces; this etching process has been optimized carefully for good device performance.[33] The Cr masks were removed by etching in 35 wt % HCl aqueous solution. Subsequently, patterned Cr/Au (thickness, 2/30 nm) contacts were deposited onto both types of samples (rough and smooth) by electron beam evaporation (steps, III−V in Figure 1a). After liftoff, the devices were treated by rapid thermal annealing at 500 °C for 3 min to form better electrical contacts. The back Si substrate with a measured resistivity of about 15 Ω·cm served as the gate electrode. The final devices with a typical optical microscopy image shown in Figure 1b have the configuration of a Si nanomembrane, which acts as an electrical channel (10−40 μm in width and 10−100 μm in length), connecting the drain and source electrodes. The devices were connected to the chip holder (Spectrum, CSB02491) by Al wires. The measurements were carried out using a semiconductor parameter analyzer (Agilent, 4156C) and a test fixture (Agilent, 16442B) at room temperature. During the measurements, the source electrode was grounded and as the light source we used a conventional room fluorescent lamp with the intensity calibrated by a laser power meter (Coherent Inc., FieldMaxII-TO). The atomic force microscopy (AFM) images were taken on a Veeco DI3100 atomic force microscope. In addition, Al_2O_3 and HfO_2 films deposited by ALD (Cambridge Nanotech Inc., Savannah-100) were used to investigate the effect of surface conditions on the rough Si channel.

Figure 1c shows the normalized current (I_{DS}, divided by the channel width) versus bias voltage (V_{DS}) curves of the rough Si nanomembrane probed in the dark and under light illumination. Figure 1d shows the same measurements for the smooth Si nanomembrane. The gate voltage V_G was set at 0. For $V_{DS} < 0$, the $I_{DS}-V_{DS}$ characteristics in the dark

and under light illumination are similar in both samples. In contrast, for $V_{DS} > 0$, the $I_{DS}-V_{DS}$ characteristic changes dramatically in the rough Si nanomembrane compared to that in the smooth one. In the rough Si nanomembrane, as the bias voltage increases from 10 to 20 V, the current across the channel is below 0.03 μA/μm in the dark; however, it increases rapidly from 1.3 to 10.3 μA/μm under light illumination. In the smooth Si nanomembrane, there is not rectifying behavior in the dark; upon illumination, the device exhibits a slight commonly observed photoresponse. These results indicate that roughening the surfaces suppresses carrier transport in a Si nanomembrane with positive bias voltages and this suppression can be overcome by illumination. As indicated by the AFM images (the corresponding insets in Figures 1c and 1d), the roughening treatment produces many ridges and valleys on the Si nanomembrane surfaces, which we identify as the origin for carrier suppression. One might argue that the effects are due to the Cr patterning, because Cr might diffuse into the rough Si nanomembrane and cause the observed effects. To rule this out, we used 20 nm thick SiO_2 masks deposited by electron beam evaporation to create rough Si nanomembranes and realize similar effects.[34]

Importantly, we found that the high conductive state activated by light persists for a long time (on the order of days) after the light is removed (Figure 1e). The drain voltage was 20 V and the gate voltage 2 V. As the device is exposed to light, the current across the rough Si channel jumps from 0.01 to 9 μA/μm and then decreases gradually, well fitted by $\ln(I/I_0) \propto -(t/\tau)^{\beta}$ with $\beta \approx 0.59$ and τ on the order of one day or more, where I is the current, I_0 is the maximal current after light illumination, t is the time, τ is the characteristic time constant for the decay of the photocurrent, and β is the decay exponent. In Si-based materials reported previously, the highest τ value is several hundred seconds to the best of our knowledge.[35] When the device is put into the dark again, the current drops slightly due to the suppression of the normal photoconductivity and then decreases very slowly; however, it still stays at a high-current state for days, maintaining the PPC effect. For comparison, the photoresponse of the smooth Si nanomembrane exhibits usual behaviors, as shown in the inset of Figure 1e. Interestingly, the persistent photocurrent of the rough Si nanomembrane can be adjusted by gate voltages (Figure 1f) and can be simply turned off by removing the bias voltage (or by applying a large positive gate voltage afterward). Previously, it was necessary to keep post-test samples in the dark environment for a sufficiently long time to be ready for the next measurement, which made sure the observed decrease of the current was due to the photocurrent decay.[36] From left to right in Figure 1f, the gate voltage decreases from 5 to −5 at 1 V steps and the bias voltage is 20 V. The initial dark current lies at about 0.03 μA/μm, while the persistent photocurrent changes at a level of about 10 μA/μm. The current after light exposure decreases with increasing gate voltage, indicating hole transport in the rough Si nanomembrane.[37]

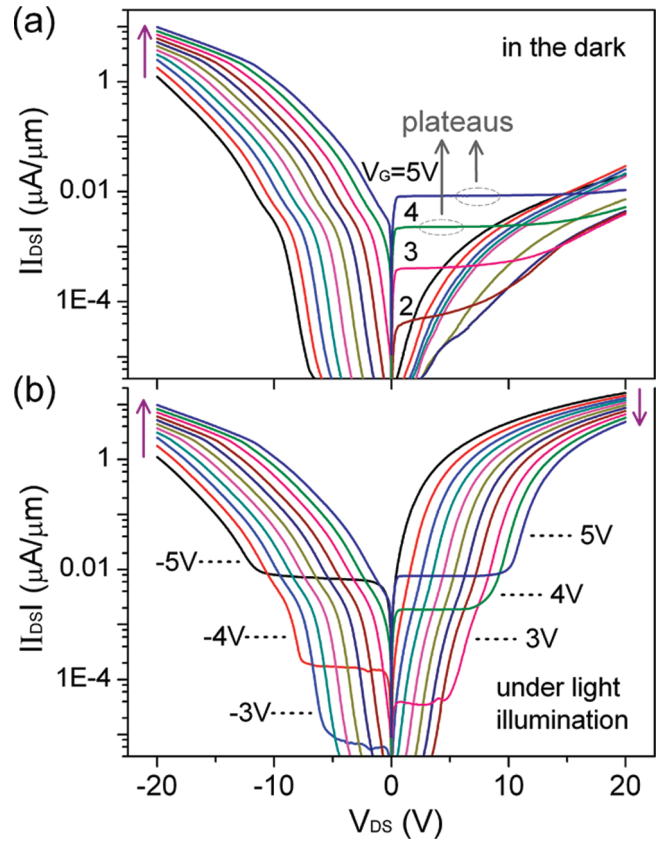

Figure 2. Typical $I_{DS}-V_{DS}$ curves of rough Si nanomembranes (a) in the dark and (b) under light illumination. Along the direction of the purple arrows, V_G increases from −5 to 5 V at steps of 1 V.

Table 1. Threshold Voltages of Rough Si-Nanomembrane Devices at Different Gate Voltages under Light Illumination

V_G (V)		−2	−1	0	1	2
V_{DS} (V)	$V_{DS} < 0$	−5.3	−4.3	−3.3	−2.35	−1.4
	$V_{DS} > 0$	1.1	1.9	2.75	3.5	4.25

To gain further insight into the properties of rough Si nanomembranes, $I_{DS}-V_{DS}$ characteristics at different gate voltages were measured in the dark (Figure 2a) and under light exposure (Figure 2b). V_G increases from −5 to 5 at 1 V steps along the direction of the purple arrows. Under dark conditions, and even for $V_G = -5$ V, which means hole accumulation in the channel, the current is still low at large positive bias voltages, indicating a strong suppression of hole transport. After exposure to light, the device exhibits ambipolar behavior: the channel is n-type for negative voltages and p-type for positive voltages. Such ambipolar behavior, which is usually observed in Schottky barrier field effect transistors,[38−41] indicates that the drain and source contacts of our devices are Schottky type. This is demonstrated by the presence of threshold voltages summarized in Table 1, by defining the threshold condition as the voltage at which the channel current is much higher than the leakage current (for instance here, the channel current is higher than 3×10^{-5} μA/μm and the leakage current lower than 6×10^{-6} μA/μm). In addition, some plateaus, indicating current saturation, appear in the transport data. As will be discussed, these plateaus are caused by the injection of carriers from

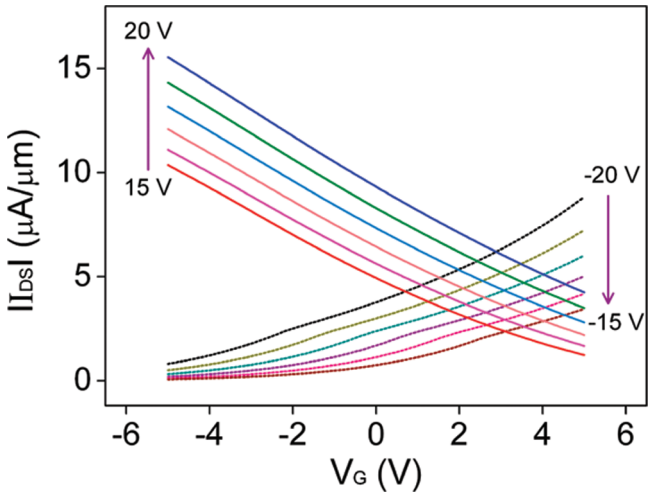

Figure 3. $I_{DS}-V_G$ plots of rough Si nanomembranes at different bias voltages. Along the direction of the arrows, the bias voltage V_{DS} changes with 1 V steps.

the source contact by thermionic emission when the Schottky barrier is lowered by the gate voltage.

The well-defined ambipolar behavior is further manifested by $I_{DS}-V_G$ results in Figure 3. Along the arrow direction, the bias voltage V_{DS} changes with 1 V steps. For negative V_{DS}, the current increases with increasing V_G (Figure 3, dashed lines), exhibiting an n-type behavior; for positive V_{DS}, the current decreases with increasing V_G (Figure 3, solid lines), hence exhibiting a p-type behavior.

The formation of Schottky contacts, as indicated by the ambipolar transport characteristics, is further supported by analyzing the band edge alignments of the Si nanomembranes and the drain and source contacts. Boron-doped Si with a resistivity of 10 Ω·cm corresponds to a doping level N_A of about 10^{15} cm^{-3}.[42] At 300 K, the intrinsic carrier concentration N_V of Si is approximately 10^{10} cm^{-3}.[37] In this nondegenerate case, the difference between the Fermi level E_F and the valence band E_V can be estimated by $E_F - E_V = -k_BT \times \ln(N_V/N_A) \approx 0.3$ eV, where k_B is the Boltzmann constant and T the temperature.[34] Accounting for the electron affinity of 4.05 eV for Si[37] and the work function of 4.83 eV for Au,[43] Schottky contacts form. Note that the Si nanomembrane channel has a length of a few tens of micrometers and a thickness of about 27 nm; it is thus expected that the drain voltage has a minor effect on the Schottoky barrier at the source contact.[44−47] Band edge alignments are proposed, as illustrated in Figure 4, which can well explain the transport characteristics of the device under light illumination in Figure 2b.

When negative voltages are applied to the drain contact, as shown in Figure 4b, the band edges move upward in comparison to the original case in Figure 4a. At low voltages, the barrier Φ_e is too high for an effective injection of electrons into the channel, and the current is low. With increase in voltage, Φ_e is lowered and electron injection is easier. After a threshold voltage is reached, the current increases rapidly and this n-type transport is determined by the density of free electrons in the channel, which can be

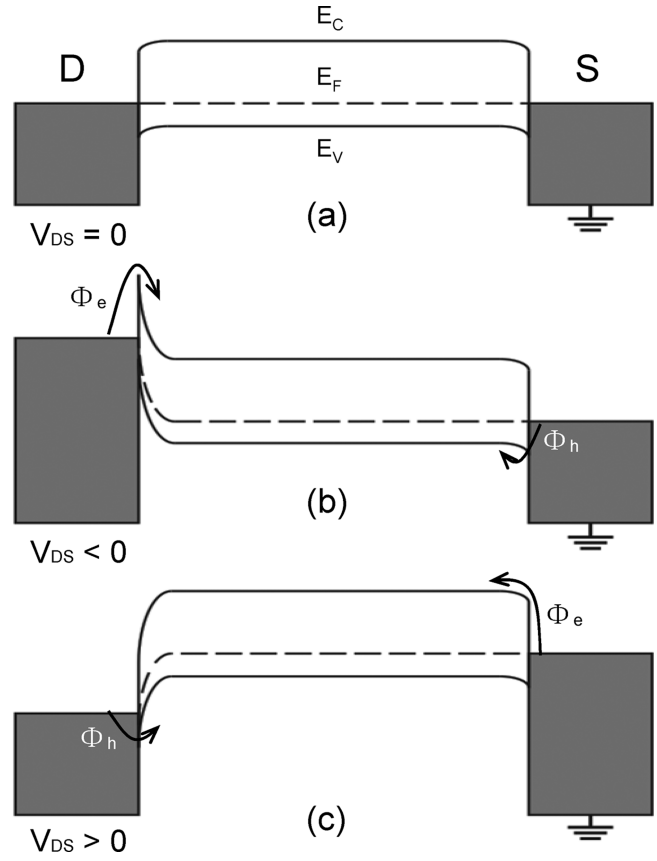

Figure 4. Band edge alignments of the device for (a) $V_{DS} = 0$, (b) $V_{DS} < 0$, and (c) $V_{DS} > 0$. E_F is the Fermi level, E_C is the conduction band edge, E_V is the valence band edge, Φ_e is the electron injection barrier, and Φ_h is the hole injection barrier.

controlled by the gate voltage. In contrast, during this process, the injection of holes at the source contact is difficult due to the barrier Φ_h. Similar arguments hold for positive voltages as displayed in Figure 4c. The magnitude of the currents at the drain, source, and gate electrodes, as denoted by $|I_{drain}|$, $|I_{source}|$, and $|I_{gate}|$, respectively, are analyzed under light illumination, as shown in Figure 5. The drain voltage V_{DS} is −7 to 7 V and the gate voltage is 0. For V_{DS} in the range of −2 to 1.8 V, the gate leakage current is comparable to the channel current and the device is off. When the device is on, $|I_{gate}|$ decreases a lot. After that, the channel current increases exponentially with increase in $|V_{DS}|$; for negative V_{DS}, $I \approx 1.02 \times 10^{-9} \times \exp[(|V|-3.3)/0.29]$, and for positive V_{DS}, $I \approx 1.89 \times 10^{-10} \times \exp[(V-2.2)/0.30]$, indicating thermionic emission consistent with Figure 4.

There are two special features observed in the curves in Figure 2b. (1) For $V_{DS} < 0$ and $V_G = -5$, −4, or −3 V, the plateaus, that is, current saturation, appear at midlevel voltages; (2) for $V_{DS} > 0$ and $V_G = 3$, 4, or 5 V, plateaus also appear. The case (1) can be understood from Figure 4b. V_G of −5 V will shift E_F very close to E_V, thus the injection barrier of electrons Φ_e at the drain contact increases, in contrast to that of holes Φ_h, which decreases at the source contact. At low voltages, electrons are not efficiently injected into the channel due to the high barrier Φ_e, and the current could be mainly determined by the injection of holes at the source. The barrier Φ_h at the source contact depends weakly

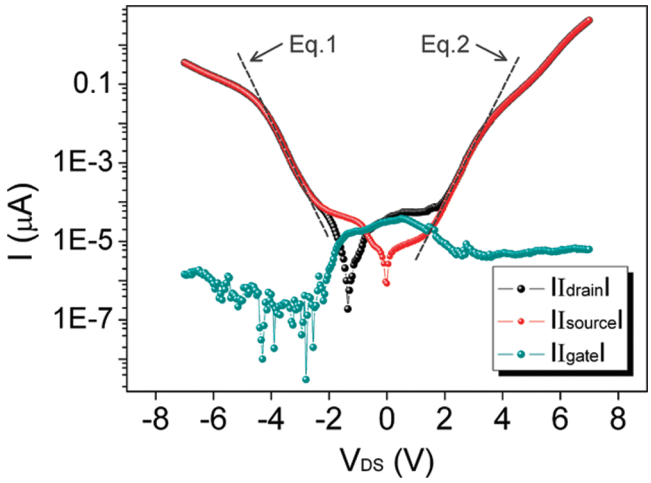

Figure 5. The magnitude of recorded drain, source, and gate currents, denoted by $|I_{drain}|$, $|I_{source}|$, and $|I_{gate}|$, respectively, of the rough Si nanomembrane for a drain voltage V_{DS} of −7 to 7 V and a gate voltage V_G of 0 under light illumination. The dashed lines are fitted curves; eq 1, $I \approx 1.02 \times 10^{-9} \times \exp[(|V|-3.3)/0.29]$; eq 2, $I \approx 1.89 \times 10^{-10} \times \exp[(V-2.2)/0.30]$.

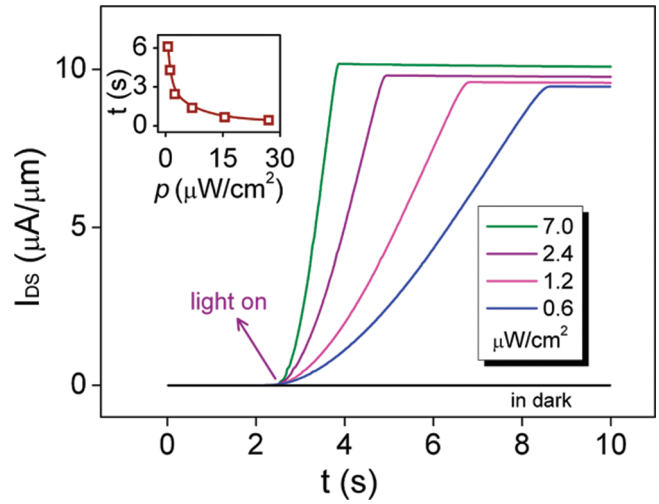

Figure 6. Current response of rough Si nanomembranes at different light intensities with blue, magenta, purple, and olive corresponding to 0.6, 1.2, 2.4, and 7.0 μW/cm^2, respectively. The black curve measured in the dark is shown for comparison. The drain voltage is 20 V and the gate voltage is 0 V. The upper inset is a plot of the response time t of the photocurrent vs. the light intensity p.

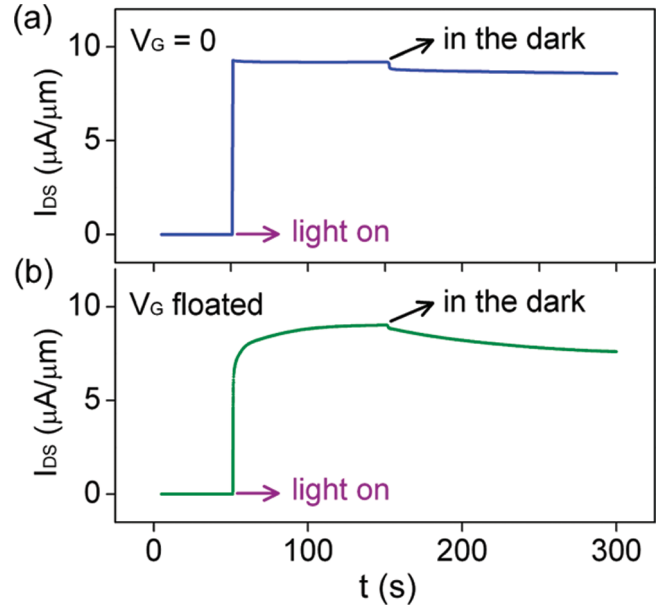

Figure 7. PPC measured (a) with grounded gate and (b) without gate. The drain voltage is 20 V. The measurements were performed under the same illumination conditions.

on the drain voltage, leading to the formation of the current plateau, which is absent in the dark and indicative of hole transport suppression. This plateau vanishes when the barrier Φ_e is lowered at large voltages and electron transport dominates. In the case of $V_G = -4$ or -3 V, the changes of Φ_e and Φ_h are smaller. Thus the current at the plateau, which is determined by the hole injection barrier Φ_h, is lower and this plateau disappears quicker with increase in voltage. A similar scheme can be used to explain the plateaus in case (2) by considering the mediation of the electron injection barrier Φ_e at the source contact by the gate voltage (Figure 4c), and the plateaus in the dark for $V_{DS} > 0$ and $V_G = 2$, 3, 4, and 5 V (Figure 2a) as well.

The above analyses, which reveal the transport properties of the rough Si nanomembranes under light illumination, cannot explain the suppression of hole transport in the dark, as revealed in the right part of Figure 2a (the current is low) and the left part of Figure 2a (the plateaus due to hole transport disappear). To explore this suppression, we measured the current response at different light intensities (Figure 6) and the PPC effect with and without a gate (Figure 7). We find that the current across the rough Si channel responds more rapidly if the illumination intensity is higher. However, the persistent photocurrent depends weakly on the light intensity. In order to measure the response time, we used light with intensities on the order of μW/cm^2. With increasing intensity p, the response time t decreases exponentially and can be fitted roughly by $t \approx 8e^{-p/1.7} + 0.5$, as shown in the upper inset of Figure 6. We notice that the response curves start with a slow increase, followed by a rapid increase, which is opposite to the response of typical photoconductive detectors.[48,49] In addition, by using a gate electrode even if it is grounded ($V_G = 0$), the photocurrent increases rapidly (Figure 7a) and the time resolution is limited by the shutter opening time (0.5 s); in contrast, without a gate electrode the photocurrent increases slower (Figure 7b) and follows a more conventional response behavior. After using the gate, we suppose that an electric field accelerates the response time of the photocurrent, which means that it speeds up the release of suppressed holes upon light illumination.

In order to describe the PPC effect of the rough Si nanomembranes in depth, the following five characteristic features are revealed: (1) the PPC effect only happens in the case of hole injection; (2) the suppression of hole transport in the dark is released upon illumination, which gives rise to the PPC effect; (3) the gate voltage can modulate the hole density in the channel and thus the persistent photocurrent; (4) by using the gate, the response time of the photocurrent is short and decreases exponentially with

increasing the light intensity; (5) without using the gate, the photocurrent increases slower.

On the basis of the structure of our devices, there are two factors that we should check, fixed oxide charges in the gate dielectric, which are known to affect the threshold voltages and transport behaviors of SOI-based field-effect transistors,[50,51] and the thinning of the Si nanomembranes after etching. The fixed oxide charges mainly affect the field effect of the gate voltage on the transistor channel, which is very similar to the charges in a floating gate of a floating gate field-effect transistor.[52] If it is critical, it should affect both electrons and holes. However, in our experiments, we find out that (1) without using a gate the PPC effect can still be realized; (2) the PPC effect only occurs for holes; and (3) fixed oxide charges should affect the original smooth Si nanomembranes, where no PPC effect is observed. These results do not support the interpretation that fixed oxide charges are the main reason for the PPC effect. Thinning of the Si-nanomembrane channel should affect the transistor characteristics. It should also affect electrons, not just holes. We cannot fully rule out the thinning effect but it is not the main factor for the observed PPC effect.

Over the years, the PPC effect has been mostly observed in III−V and II−VI semiconductor compounds due to insufficient crystalline perfection and has been closely related to deep defect levels.[23−26] There are two main models that have been taken to explain this. The first suggests atomic scale microscopic barriers existing around defect centers with large lattice relaxation, which applies well to compounds such as $Al_xGa_{1-x}As$.[23,24] The other explanation stems from the spatial separation of photoexcited electrons and holes by macroscopic barriers due to band bending at the surface or interface.[25,26] As for Si, previously the PPC effect has been observed in four kinds of structures, compensated a-Si:H,[53] porous Si,[31] doping modulated a-Si:H superlattices,[35] and p-type bulk Si covered by an n-type surface layer.[30] The PPC effect is mainly interpreted in terms of creation of metastable defects due to illumination[53] or spatial separation of carriers of different signs.[30,35]

Our devices with rough Si nanomembranes have double Schottky contacts; hence the transport is controlled by one type of carrier, as shown in Figures 2b and 3. In the dark, hole transport in the rough Si nanomembrane channel is suppressed and the release of this suppression upon illumination results in the observed PPC effect. The Si nanomembranes are single crystalline. Therefore, it is reasonable to rule out large lattice relaxation, which is usually applied to imperfect compounds,[23,24] and creation of metastable defects, which is usually relevant for a-Si:H.[53] In single-crystal p-type bulk Si, the PPC effect has been observed by creating a thin diffusion-generated n-type layer on the surface.[30] Upon illumination, recombination of photogenerated holes and electrons is precluded by their spatial separation at the p-n junction. The holes remain mobile in the p-type bulk Si, generating the persistent conductivity after the illumination is terminated.[30] In this case, creating an n-type layer elongates the lifetime of the excess holes. In our case, roughening the surfaces suppresses the hole transport. On the basis of the presence of many ridges and valleys (Figure 1c, inset) in our rough Si nanomembranes compared to the original smooth surface (Figure 1d, inset), we believe that a rough surface can generate similar barriers for excited charge carriers, that is, holes here, and induces the persistent photocurrent. Hence it is reasonable to propose that the created rough surfaces immobilize holes in the Si nanomembranes, that is, localize holes or separate holes from electrons spatially; light can activate the confined holes and thus induce the observed PPC effect.

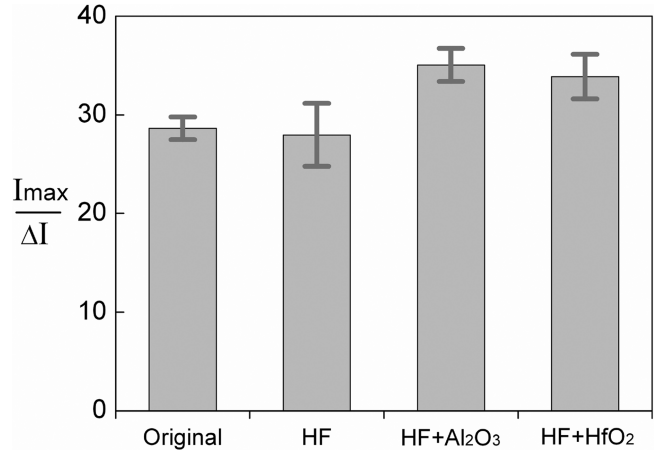

Figure 8. Bar graph illustrating the PPC effect in the rough Si nanomembranes with various surface treatments. The height of each bar represents the ratio ($I_{max}/\Delta I$) between the maximum photocurrent (I_{max}, as marked in Figure 1e) and the current drop (ΔI). From left to right, the bars correspond to the original, HF-treated, Al_2O_3-coated, and HfO_2-coated rough Si nanomembranes, respectively. The coatings with a thickness of 10 nm were realized by ALD.

Finally, a bar plot (Figure 8), which documents the surface influence on the PPC effect via oxide coatings, is used to exclude surface adsorption or desorption. The height of each bar represents the ratio ($I_{max}/\Delta I$) between the maximum photocurrent (I_{max}, as marked in Figure 1e) after illumination and the current drop (ΔI) when the device is put into the dark again, which we consider as the current change due to the normal photoconductivity. The first bar corresponds to original rough Si nanomembranes. For eight devices with different channel lengths (10−100 μm) and widths (10−40 μm), it is found that $I_{max}/\Delta I$ changes slightly. For comparison, the following three types of surface treatments are used: (1) removing the native oxide layer on the surface of the rough Si channel by HF etching; (2) removing the native oxide layer and immediately growing a 10 nm thick Al_2O_3 film by ALD; (3) removing the native oxide layer and immediately growing a 10 nm thick HfO_2 film by ALD. The values of $I_{max}/\Delta I$ are shown in bars 2, 3, and 4 for cases (1), (2), and (3), respectively. The HF-treated samples (bar 2) are similar to the original samples (bar 1) except for an increased error bar. The oxide-coated samples (bars 3 and 4) have slightly higher ratios of $I_{max}/\Delta I$. However, there is no degradation of the PPC effect after coating, which rules out surface defects or contaminations, as well as gas adsorption and desorption.[49,54]

In summary, we have observed a giant PPC effect in rough Si nanomembranes, which is interpreted in terms of the

introduction of hole-localized regions in the Si nanomembranes by surface roughening and has potential applications such as bistable optical switches[19,20] and radiation detectors.[21,22] Our findings manifest a giant PPC effect achieved by roughing the surfaces of Si nanomembranes, which emphasizes a new feature of rough surfaces in nanoscale structures. Our work here, together with other examples on enhanced thermoelectric performance of rough Si nanowires,[7] suggests that certain interesting physical and chemical phenomena could become more significant in comparison with the bulk, by introducing rough surfaces in nanostructures.

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